Titan2 Series FPGA Clock Resource (Clock) User Guide

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Document version revision record

Version number	Release date	Revision history
V0.1	2020/10/16	Initial version
V0.2	2020/12/24	1. Modify Figure 2, so that the global clock can only pass through the HCKB to the logic; 2. Change the output clocks of the source synchronisation modes Figure 56 and Figure 75 in Chapter 2 from buf to clkbuf; 3. Chapter 2, APB Configuration Interface, is divided into three subsections, subsection, 5.2 adds a detailed functional description of the registers, and subsection, 5.3 adds a description of the configuration constraints.
V0.3	2020/12/31	1. Remove all coordinates containing GPLL/PPLL from all diagrams. 2. Modify the description of the interpolated phase shift in chapter II, subsection 6.8, by adding a formula for the number of degrees of adjustment and a formula for the number of degrees of adjustment of the step relative to the output clock. 3. Modify the global clock connection diagram in Figure 5 , the global clock can only pass through HCKB and then to the logic; 4. Remove the PPLL6.7 interpolation phase shift DPS configuration interface description, PPLL does not have this function.
V0.4	2020/3/23	1. General introduction: clock resources are divided into 4 subsections, adding an overview of clock buffer, and overview of PLLs , and clock connection overview to 3 subsections ; 2. Detailed introduction: Add all clock resources (input clock pins, clock buffer and PLL) input/output sources and driveable resources, and specify the scope; Detailed introduction: add the input clock pin layout rule table in section 1.2 and add sections 2.2,3.2,4.2,5.2,6.2, and 6.3; 3. GTP_GPLL: Add section 3.1 GTP_GPLL detailed interface description, section, 7 GTP_GPLL configuration constraints and add section 8.4 Cascading between GPLLs; 4. GTP_PPLL: Add the detailed interface description of GTP_PPLL in section 3.2 , the configuration constraints of GTP_PPLL in section, 7 and the cascading between PPLLs in section8.4.
V0.5	2020/4/29	1. GPLL and PPLL feedback output clock names changed to CLKOUTF/CLKOUTFN; 2. Modify GPLL/PPLL loop bandwidth description; 3. Added BUFGMUX/BUFGMUX_E1/BUFGMUX_E2 input clock requirements description.
V1.0	2020/6/10	1. Section "Clock Connection Overview, table 2 , PPLL supplemented CLKOUT4, HSSTHP reference clock name changed to be consistent with GTP; 2. Modify the input clock source and output connection diagrams and related descriptions in the"Horizontal Clock Network", "Regional Clock Network", "IO Clock Network", "Cross-Regional Clock Network"and"PLL Clock Resources"sections; 3. Modify the phase description of GPLL and PPLL and add examples; modify the PPLL duty ratio port description error; add the input clock reset scene description in section 6.1 ;
V1.1	2020/6/20	1. Modify the annotation of the clock network GTP timing diagram, and change the "timing diagram" from 1 to "timing diagram"; 2. Add the IO clock GTP parameter description table18, modifyFigure 29, remove the parameter configuration port in the timing diagram, and modify Figure 24, RCKB input SRB expression error; 3. Modify GPLL Figure 47 and PPLL Figure 70, and supplement external feedback instructions; 4. Supplement the content of GPLL and PPLL including the description of the principle of programmable output frequency in Section 6.5 the description of loop bandwidth selection in table 23 and table 35, the description of which parameters need to be configured for phase adjustment, and the description of how to achieve fractional frequency division;

Glossary

Abbreviations	Full Spelling
USCM	User Select Clock Module
SRB	Signal Relay Block
GCLK	Global Clock
RCLK	Regional Clock
HCLK	Horizontal Clock
HCKB	Horizontal Clock Buffer
RCKB	Regional Clock Buffer
MRCKB	MIT-Region Clock Buffer
GMCLK	Global Multiplex Clock
GSCLK	Global Single Clock
GTP	General Technology Primitive
HSSTHP	High Speed Serial Transceiver High Performance

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1. General introduction

(1) The overall introduction of the clock

1. Overview of Clock Resources

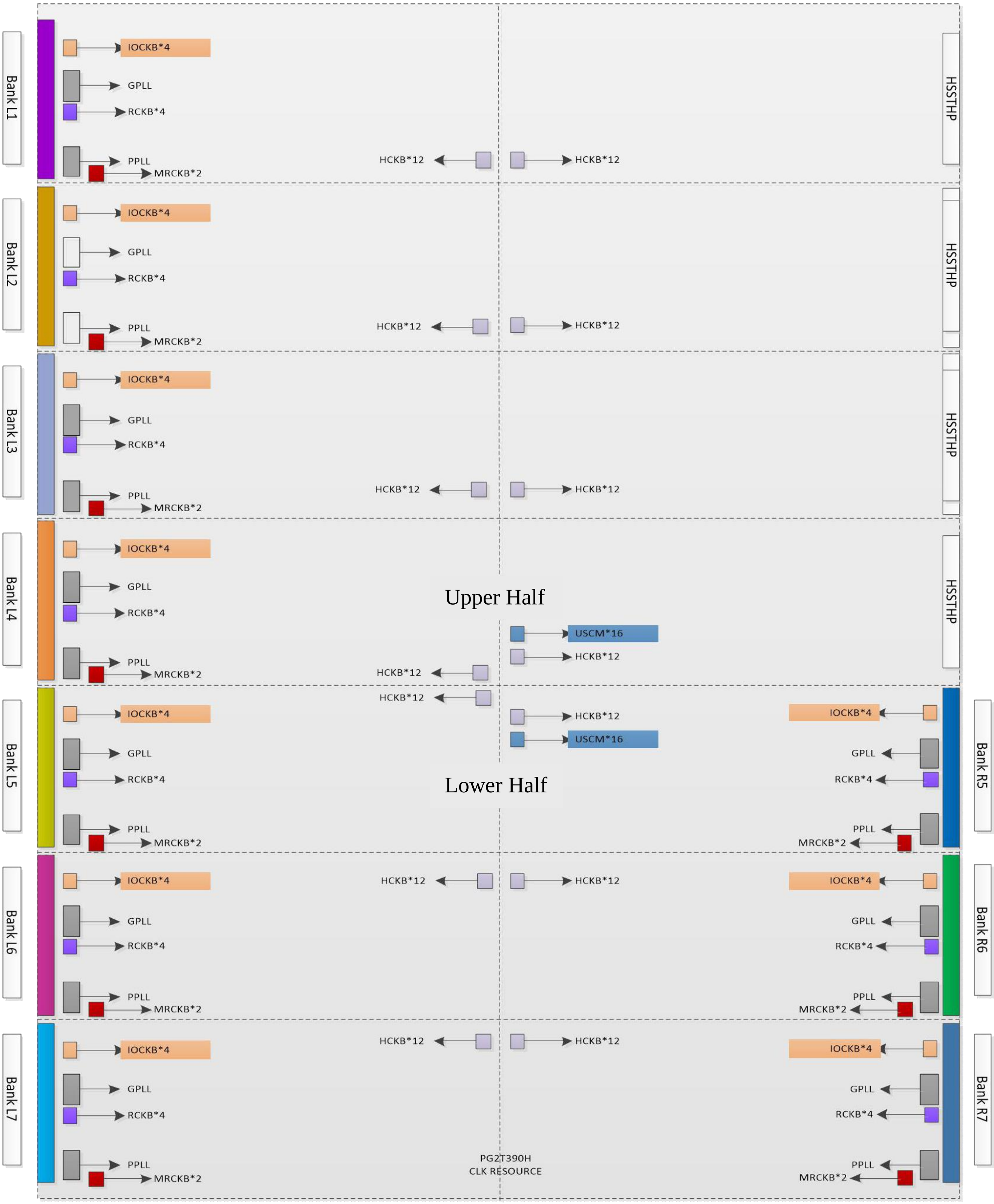


Figure 1 PG2T390H Clock Resource Maps

Titan2 series products provide a wealth of on-chip clock resources, of which the PG2T390H clock resources as shown in Figure 1, including: 32 GLOBAL CLK, the entire device is divided into the upper half, the lower half of the two parts, each part of the 16 independent GLOBAL CLK network. Region-based REGIONAL CLK, the entire device is divided into multiple regions, each Region has 4 REGIONAL CLK networks. IO CLK for high-speed interface applications, with seven IO CLK networks on the left side of the device (Top View) and four IO CLK networks on the right side of the device (Top View). There are also HORIZONTAL CLK clock resources for horizontally adjacent clock regions and cross-clock region clock resources for vertically adjacent clock regions.

The PG2T390H provides 10 PPLLs and 10 GPLLs to meet the user's needs for frequency variation and phase adjustment. The GPLLs provide more frequency divisions and functions than the PPLLs, which provide clocks for DDR, etc. The PG2T390H provides 10 PPLLs and 10 GPLLs to meet user needs for frequency variations and phase adjustments.

The overall clock resources of the chip are shown below:

- The PG2T390H chip has 32 GLOBAL CLOCKS, with 16 GLOBAL CLOCKS on the top and bottom of the chip.
- The PG2T390H chip has 40 REGION CLOCKS, except for the 4 REGIONS where the HSSTHP is located, each REGION has 4 REGION CLOCKS.
- The PG2T390H chip has 168 HORIZONTAL CLOCKS, 12 HORIZONTAL CLOCKS in each REGION.
- The PG2T390H chip has 40 IO CLOCs, 4 IO CLOCs per IO BANK.

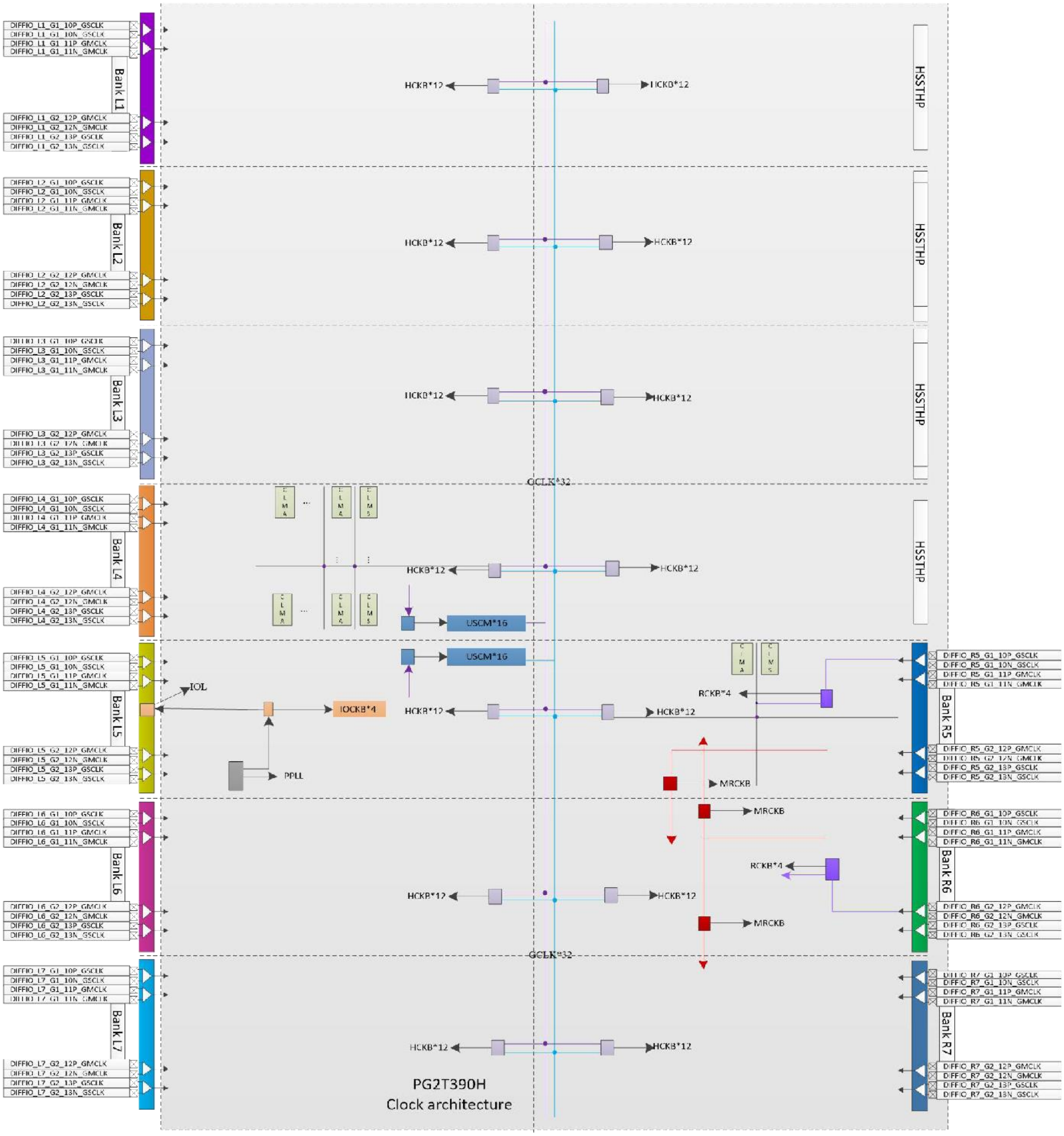


Figure 2 PG2T390H Clock Architecture Diagram

Figure 2 shows the PG2T390H clock architecture. The GLOBAL CLOCK, driven vertically by the USCMs, provides the synchronous clocks for the synchronous logic units of the entire chip, of which 16 USCMs are located in the upper half of the chip, and the other 16 USCMs are located in the lower half of the chip. As can be seen from the above diagram, the clock pins allow the user's clock to:

- Same upper/lower half of USCM.
- HCKB of the same or neighboring horizontal area, through HCKB to the clock network of the same area.
- RCKB of the same region, via RCKB to the regional clock network.
- MRCKB of the same region (only the input clock pin GMCLK is supported) to clock the upper and lower clock regions adjacent to the current clock region.
- IOCKB of the same area, providing clock for IOL of the same area through IOCKB.

2. Clock buffer overview

1. Overview of the global clock buffer

The PG2T390H device has a total of 32 USCMs, and the clock source reaches the global clock network through the USCM, and each region supports up to 12 global clock networks, which share the clock network in the same region with the 12 horizontal clocks.

USCM has the following characteristics:

- It can realize the dynamic enable control of the input clock.
- Provide selection function, which can realize dynamic switching of two clock sources.
- Support cascading between adjacent USCMs, which can be realized by using two global clocks GTP to cascade with each other.

2. Horizontal clock buffer overview

Individual zone horizontal clock networks can be reached via HCKB with dynamic enable control, each zone supports up to 12 HCKBs to 12 independent horizontal clock networks.

3. Overview of regional clocks, IO clocks, and cross-regional clock buffers

The area clock network and IO clock network can be reached through RCKB and IOCKB, respectively, which can be used in conjunction with MRCKB to span three adjacent vertical areas with the following characteristics:

- Supports up to 4 RCKBs and 4 IOCKBs per region.
- RCKB drives the same area of IOL (IO logic) and FPGA internal logic resources, and has a frequency divider function that can be used as a frequency divider.
- IOCKB can only drive IOLs in the same region.
- The RCKB/IOCKB output clock is used as the interface clock for ISERDES/OSERDES, which enables source synchronization across frequency domain clocks without consuming additional logic resources.
- Through MRCKB, the same clock source can reach the 3 vertically neighboring area clock networks and the IO clock network.

4. Clock GTP Overview

In practice, if the external clock comes in from the clock pin to directly drive the FPGA logic, the software will automatically let the clock go to the global clock network; if the clock is directly used as an input to the PLL, and the clock pin and the PLL are on the same side, the clock input to the PLL will be reached through the PLL's dedicated clock path; for the regional clock and the IO clock, it is necessary to routinely use the corresponding GTP to let the clock reach the regional clock network and the IO clock network; if you want to use more functions with the clock buffer, such as dynamic enable of the global clock, it is necessary to routinely use the corresponding clock GTP to achieve this. For area clock and IO clock, the corresponding GTP needs to be instantiated in the code to allow the clock to reach the area clock network and the IO clock network; if you want to use more functions of the clock buffer, such as the dynamic enable of the global clock, you need to realize it by instantiating the corresponding clock GTP.

The PG2T390H device has a wide range of clocking GTP resources to meet the needs of many different clocking applications. Choosing the right clock resource can improve layout reliability, performance, and FPGA resource utilization. For some applications and designs, manual layout planning can have a significant impact on implementation.

All GTPs with global clocks can drive all resources with clocked nodes, so global clocks are most commonly used and are considered in the following cases:

- Logic that drives multiple zones as one clock.
- GTP_CLKBUFGCE with enable turns off the output clock when the logic does not need to work, which reduces the power consumption.
- When there are two input clocks, in one case, one of them is needed as an alternative, and the alternative clock can be activated when the other one is abnormal or lost, and in the other case, the two input clocks have different frequencies and need to be switched, which can be realized by using GTP_CLKBUFGMUX/ GTP_CLKBUFGMUX_E1/ GTP_CLKBUFGMUX_E2.

The GTP of the area clock corresponds to RCKB and the GTP of the IO clock corresponds to IOCKB, as shown in Table 1. The GTP of the IO clock corresponds to IOCKB, as shown in Table 1. According to the characteristics of RCKB, when all the resources are in the same region, the regional clock GTP can be exemplified in the code, and the clock source passes through the GTP and reaches the regional clock network to drive the internal logic and the IOL, and the divider function of RCKB can be used through GTP_IOCLKDIV_E2, and in some cases, GPLL/PPLL can be avoided to save the GPLL/PPLL resources. PPLL resources. In some high-speed interface logic applications, GTP with IO clock is required, e.g. GTP_IOCLKBUF output clock is used to connect to OSERDES high-speed clock interface. Cross-region clock GTP corresponds to MRCKB. If you want the clock to span vertically neighboring regions, and the input clock drives RCKB/IOCKB after passing through the cross-region clock GTP, you can realize that one clock source can drive the logic resources of three regions.

Horizontal clock GTP corresponds to HCKB, in some cases it is possible to use HCKB directly to drive the logic, it is necessary to exemplify the corresponding GTP:

- When the I/O interfaces of a design module and the internal logic resources it occupies are in the same area or in two horizontally adjacent areas.
- GPLL/PPLL external feedback input clock.
- When the module does not need to work and the driven logic is only in one area, use GTP_CLKBUFXCE with an enable terminal to turn off the clock output to reduce power consumption.
- The mapping relationship between clock GTP and clock buffer is shown in the following table:

Table 1 Clock GTP and clock buffer mapping

Serial number	Clock buffer	Clock GTP
1	USCM	GTP_CLKBUFG
2		GTP_CLKBUFGCE
3		GTP_CLKBUFGMUX
4		GTP_CLKBUFGMUX_E1
5		GTP_CLKBUFGMUX_E2
6	HCKB	GTP_CLKBUFX
7		GTP_CLKBUFXCE
8	RCKB	GTP_CLKBUFR
9		GTP_IOCLKDIV_E2

Serial number	Clock buffer	Clock GTP
10	IOCKB	GTP_IOCLKBUF
11		GTP_CLKBUFM
12		GTP_CLKBUFMCE

3. PLL Overview

Titan2 series devices have 1 GPLL and 1 PPLL in each area except the HSSTHP area, which can be used for clock frequency synthesis, clock SKEW reduction, phase adjustment, etc. PPLL has fewer functions than GPLL, and the main differences are as follows:

- Input/output frequency range, jitter and other parameter characteristics, please refer to the device data sheet "DS05001_Titan2" for details.
- In terms of interface, PPLL has no DSP interface, and the clock output interface has two fewer channels than GPLL. PPLL has an interface to provide clock for DDR PHY. For details, please refer to the system block diagram in Figure 38 and Figure 61 GPLL/PPLL overview.
- PPLL does not support: interpolation phase shift, spread spectrum output, fractional frequency division and output frequency divider cascading.

4. Overview of Clock Connections

Table 2 summarizes the input clock sources and output resources that can be directly driven by the Titan2 series FPGA clock pins and each clock buffer, and clarifies the relevant constraints. Knowing the characteristics of all clock resources is helpful for us to make better clock planning and FPGA design.

Table 2 Clock Connection Summary

Clock buffer/pin	Clock source	Outputs can directly drive resources
GMCLK, each IO bank has two pairs of differential inputs	External clock source	Same area: ➢ RCKB ➢ IOCKB ➢ MRCKB Same area or adjacent horizontal areas: ➢ HCKB Same left or right half: ➢ 1 or more GPLL/PPLL Same upper or lower half: ➢ USCM
GSCLK, each IO bank has two pairs of differential inputs	External clock source	Same area: ➢ RCKB ➢ IOCKB Same area or adjacent horizontal areas: ➢ HCKB Same left or right half: ➢ One or more GPLL/PPLL Same upper or lower half: ➢ USCM

Clock buffer/pin	Clock source	Outputs can directly drive resources
USCM	Same upper or lower half: ➢ GSCLK and GMCLK ➢ GPLL and PPLL ➢ HCKB(HSSTHP1~ HSSTHP4 not support) ➢ RCKB ➢ SRB(Not recommended) ➢ Adjacent USCM ➢ HSSTHP (the table HSSTHP clock)	➢ Driving GPLL/PPLL via HCKB ➢ Adjacent USCMs in the same half ➢ Any logic unit that has a clock pin ➢ 4 HSSTHPs in the upper half (the tableHSSTHP clock) ➢ All HCKB ➢ CLMA control signal
HCKB	Same area and adjacent horizontal areas: ➢ GSCLK and GMCLK ➢ PPLL and GPLL ➢ HSSTHP (the table HSSTHP clock) whole chip: ➢ upper half/lower half USCM ➢ SRB (not recommended)	Same area: ➢ GPLL/PPLL ➢ HSSTHP (the table HSSTHP clock) ➢ Any logic unit that has a clock pin. ➢ I/O logic (IOL) Same half: ➢ USCM
RCKB	Same area: ➢ GSCLK and GMCLK ➢ PPLL and GPLL CLKOUT0~3/N ➢ SRB Same and vertically adjacent regions: ➢ MRCKB	Same area: ➢ GPLL/PPLL ➢ Any logic unit that has a clock pin ➢ I/O logic (IOL) same upper or lower half: ➢ USCM
IOCKB	Same area: ➢ GSCLK and GMCLK. ➢ PPLL and GPLL CLKOUT0~3/N Same and vertically adjacent regions: ➢ MRCKB	Same area: ➢ I/O Logic (IOL)

Clock buffer/pin	Clock source	Outputs can directly drive resources
MRCKB	Same area: ➢ MRCKB ➢ SRB	Same and vertically adjacent regions: ➢ RCKB ➢ IOCKB
GPLL/PPLL	➢ G GMCLK and GSCLK in the left or right half of the zone ➢ USCM ➢ RCKB in the same area ➢ HCKB in the same region ➢ GPLL/PPLL CLKOUT0~3/N	GPLL: ➢ CLKOUT0~3/N, CLKOUT4~6, CLKOUTF/CLKOUTFN: same half Area USCM and the same or adjacent horizontal area HCKB; ➢ CLKOUT0~3: same area RCKB and IOCKB; PPLL: ➢ CLKOUT0/N, CLKOUT1~4, CLKOUTF/CLKOUTFN: same half area USCM and the same or adjacent horizontal area HCKB; ➢ CLKOUT0~3: same area RCKB and IOCKB; ➢ CLKOUTPHY/N:DDR PHY;
HSSTHP Clock: P_TX_CLK_FR_CORE P_RX_CLK_FR_CORE	➢ USCM ➢ HCKB in the same region	N/A
HSSTHP Clock: P_RCLK2FABRIC P_TCLK2FABRIC	N/A	➢ Same upper/lower half USCM ➢ HCKB in the same region
HSSTHP reference Clock: PAD_REFCLKN_0P/0N PAD_REFCLKN_1P/1N	External HSSTHP reference clock	➢ Same upper/lower half USCM ➢ HCKB in the same region

(2) CLOCK REGION

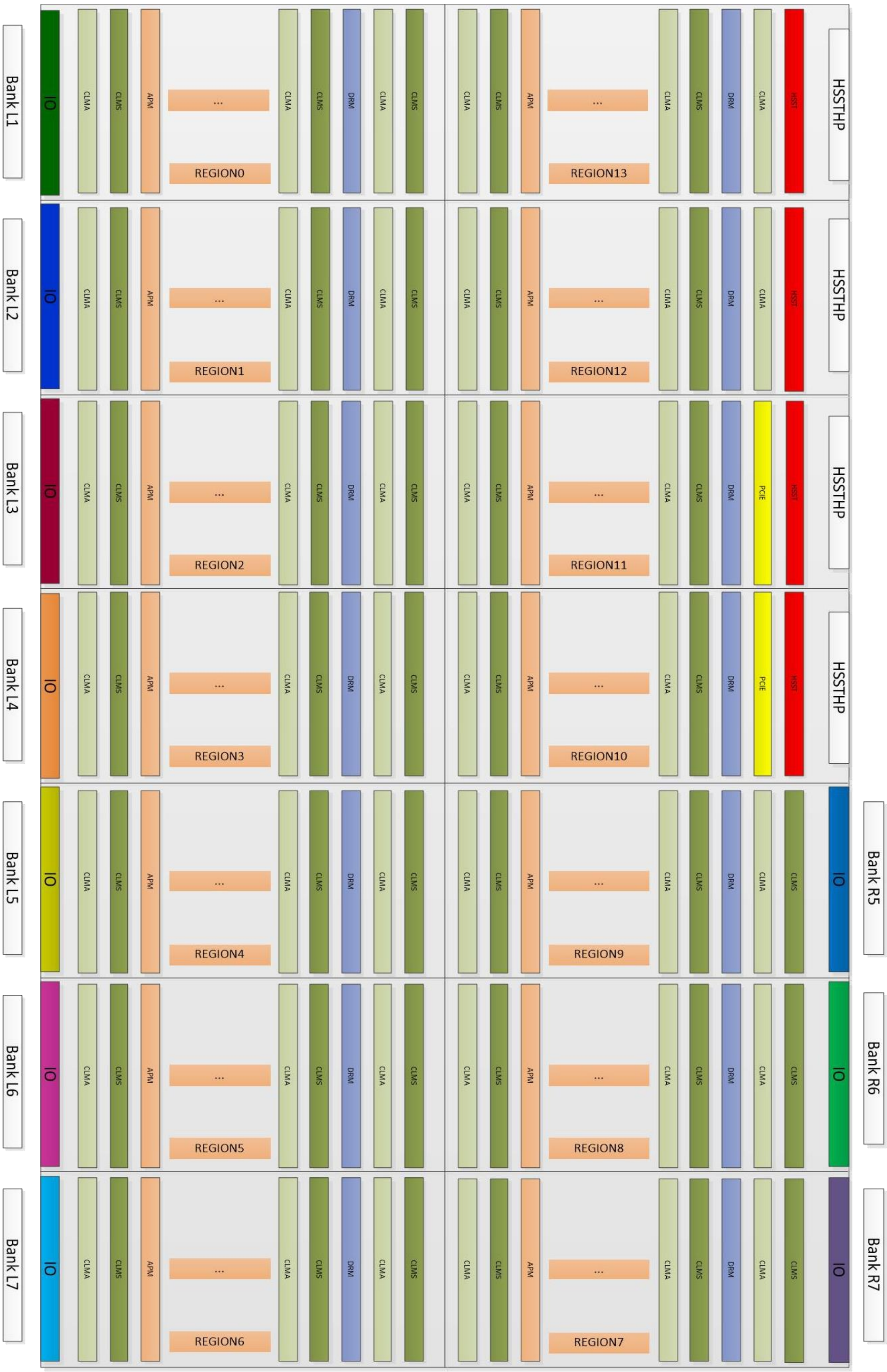


Figure 3 Clock Region Structure Diagram

The internal logic resources of Titan2 series products are distributed according to Region, and each Region is composed of a certain number of CLMA, CLMS, DRM, IO and APM columns, etc.,

and its vertical height is about 50 CLMA or CLMS and 1 IO LOGIC height, The lateral width varies according to the logic capacity of the chip. PG2T390H consists of 14 Regions, as shown in Figure 3.

2. Detailed introduction

(1) Detailed introduction of clock resources

The clock connection chapter will introduce the clock resources in Titan2 series FPGAs, and the relationship between these clock resources and IO clock ports, global, regional, horizontal, multi-regional and other clock buffers. It is for users to refer to when using.

1. Clock Pin Resources

1.1 Clock pin introduction

Titan2 series products provide IO pins GSCLK/GMCLK with clock function. Each BANK has two pairs of GMCLK and two pairs of GSCLK for users to use. It is recommended that users choose these clock pins first for clock input. Using these pins can avoid common wiring resources The interference caused by it, so as to get better clock performance. When these clock input pins are not used as clock input, they can be used as ordinary IO.

The clock IO pin GSCLK/GMCLK supports differential or single-ended use. When applied to differential signals, you need to use GSCLK_P/GSCLK_N or GMCLK_P/GMCLK_N differential pair ports. When applied to single-ended signals, you need to use GSCLK_P or GMCLK_P single-ended ports, At this time, GSCLK_N/GMCLK_N is no longer used as a clock port, but can only be used as a common IO application. The chip clock IO pin position is shown in Figure 4.

GSCLK/GMCLK can drive:

- RCKB, MRCKB (only supported by GMCLK) and IOCKB in the same region.
- HCKB in the same or adjacent horizontal regions.
- One or more GPLL/PPLL for left or right half.
- USCM of the same upper or lower half.

The input clock pin can drive one or multiple GPLL/PPLL at the same time. When the input clock pin only drives one GPLL/PPLL, it is best to be in the same area. If they are in different areas, but on the same side, The input clock will reach the clock input of GPLL/PPLL through the PLL clock tree. If they are on different sides in different regions, the clock will pass through USCM, and then pass through HCKB to reach the clock input of GPLL/PPLL.

Users need to pay attention to the difference between GSCLK and GMCLK clock input pins. It is reflected in the fact that GMCLK can be used as a synchronous clock to drive vertically adjacent clock regions through MRCKB, but GSCLK cannot. One BankL4 is shown in the figure below the connection relationship between the clock IO pins is shown.

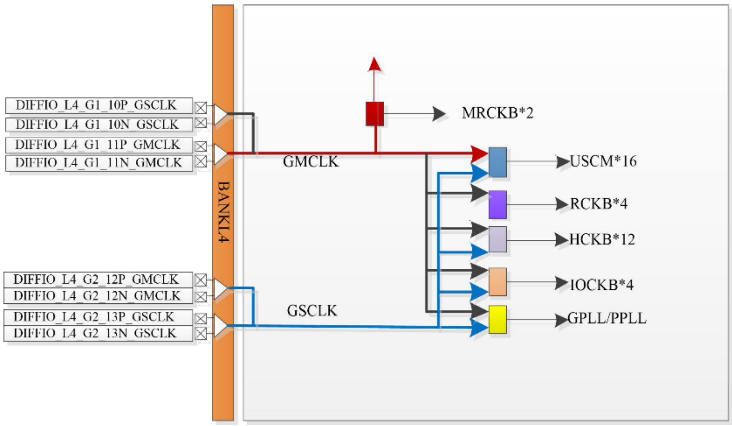


Figure 4 Clock Pin Connection Diagram

1.2 Clock input pin layout rules

When selecting a clock input pin, the following factors should be considered:

- Ensure that the input clock pins can be connected to the desired clock network resources.
- Make sure that the expected clock resource is available and not used by other clock sources. If the clock resource expected to be used by the input clock is just occupied by the GPLL output clock, the software compilation will report an error.

The specific layout rules of the input clock pins are shown in Table 3.

Table 3 Layout Rules for Input Clock Pins

Input Clock to	Clock Resource Usage and Placement Rules	Active input clock pin
I/O resources and logic resources of the entire chip	Input Clock Pins→USCM→Global Clock Tree ➢ The clock pin must be in the same upper or lower half area as USCM ➢ 16 USCMs each in the upper and lower halves ➢ Each region has 12 independent global clocks, sharing these clock networks with horizontal clocks	GMCLK or GSCLK
I/O resources and logical resources driving individual regions with HCKB	Input Clock Pin→HCKB→Horizontal Clock Network ➢ Clock pins must be placed in the same or adjacent horizontal area as HCKB ➢ 12 HCKB and horizontal clock network per region	GMCLK or GSCLK
I/O resources and driving logic resources with GPLL/PPLL	Whole chip: Input clock pins→GPLL/PPLL→USCM →Global clock tree Single area: Input clock pins→GPLL/PPLL→RCKB→Regional clock tree	GMCLK or GSCLK

Input Clock to	Clock Resource Usage and Placement Rules	Active input clock pin
	Single or horizontally adjacent regions Clock pin input→GPLL/PPLL→HCKB→Horizontal clock network Input clock to GPLL/PPLL routing rules: ➢ PLL clock tree between the same left half or right half ➢ Across the left and right half areas need to be achieved through USCM GPLL/PPLL ➢ Outside the area where the HSSTHP is located, 1 per area GPLL/PPLL	
I/O resources and driving individual region logical resources with RCKB	Input Clock Pins→RCKB→Regional Clock Tree ➢ Input clock pins must be in the same region as RCKB, I/O resources, and logic resources driven by the clock ➢ Outside the area where HSSTHP is located, each area has 4 pairs of differential clock pin input and 4 RCKB	GMCLK or GSCLK
I/O resources and logical resources of three adjacent areas driven by MRCKB	Input Clock Pins→MRCKB→RCKB→Regional Clock Tree ➢ The I/O resources and logic resources driven by RCKB must be in the same or adjacent vertical and horizontal areas as the input clock pins ➢ The RCKB driven by MRCKB must be in the same or adjacent vertical horizontal area as the input clock pin ➢ Outside the area where HSSTHP is located, each area has 4 pairs of differential clock pin input, 4 RCKB and 2 MRCKB	GMCLK only
High-speed interfaces in the same area	Input Clock Pins→IOCKB→I/O Clock Tree ➢ The input clock pin must be connected to IOCKB and the IOL in the same area ➢ 4 pairs of differential clock pin inputs, 4 IOCKB, and 2 MRCKB per region outside of the HSSTHP region	GMCLK or GSCLK
High-speed interfaces in the same and adjacent vertical areas	Input Clock Pins→MRCKB→IOCKB→I/O Clock Tree ➢ The input clock pin must be connected to IOCKB and the IOL in the same or adjacent vertical area ➢ The IOCKB driven by MRCKB must be in the same or adjacent vertical horizontal area as the input clock pin ➢ Outside the area where HSSTHP is located, each area has 4 pairs of differential clock pin inputs, 4 IOCKBs and 2 MRCKBs	GMCLK only

2. Global clock resource

2.1 Global clock network

As the driver of the global clock, the USCM provides the global clock GCLK for the synchronous logic units in the clock region.

The input sources for USCM are:

- The clock input pins of the same upper/lower half area GSCLK and GMCLK, PLL, HCKB (not supported in the area where HSSTHP is located), RCKB, SRB, adjacent USCM.
- HSSTHP output clock for upper half.

Among them, the global clock sources from PLL include: CLKOUTF, CLKOUTFN, CLKOUT0~CLKOUT4, CLKOUT0N of PPLL; CLKOUTF, CLKOUTFN, CLKOUT0N~CLKOUT3N, CLKOUT0~CLKOUT6 of GPLL.

USCM can drive:

- GPLL/PPLL
- Adjacent USCM
- Any logic unit and IOL with a clock pin
- HCKB
- HSSTHP's 4-way RX user clock, 4-way TX user clock and 2-way reference clock (see Chapter 1, Section 4, Clock Connection Overview for details).

The connection relationship of USCM is shown in the red circle in Figure 5.

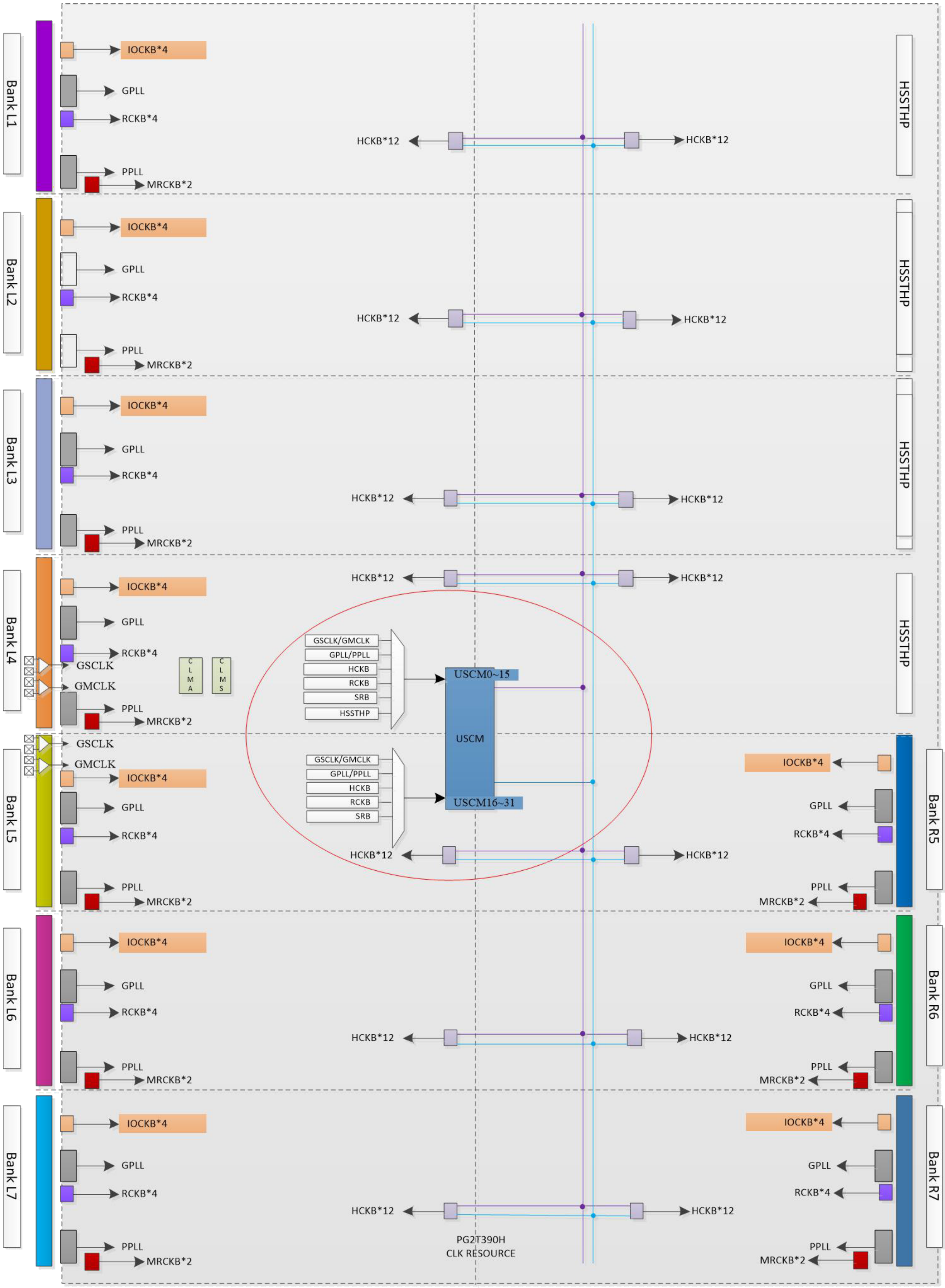


Figure 5 Connection Diagram of Global Clock

There are 32 USCMs in the whole chip. In Figure 5, the horizontal dotted line in the red circle divides the chip into the upper half and the lower half, and the vertical dotted line divides the chip into the left half and the right half. The clock input sources in the upper half can only reach the 16 USCMs in the upper half, and the clock input sources

in the lower half can only reach the 16 USCMs in the lower half. All 4 HSSTHPs are distributed in the upper half. It occupies many clock resources, and only global clock resources and horizontal clock resources can be used (priority is considered).

The clock sources of the global clock (GMCLK/GSCLK, GPLL/PPLL, HCKB, RCKB, SRB, etc.) are distributed in 14 clock regions. Each clock region can provide up to 14 clock sources for the global clock at the same time. When users use the global clock this point needs to be taken into consideration, and the location of the clock source should be reasonably arranged. In addition, each clock region has at most 12 global clock-driven logic.

2.2 Global clock GTP

Titan2 series products have abundant global clock GTP resources. One GTP will occupy one USCM. Different GTPs have different functions, such as GTP_CLKBUFGCE with enable control. The enable signal CE controls whether to output the clock. Dynamic switching of the input clock, etc.

The included global clocks GTP are shown in the table below:

Table 4 Global Clock Buffer Primitives List

Primitive	Input	Output	Control signal
GTP_CLKBUFG	CLKIN	CLKOUT	—
GTP_CLKBUFGCE	CLKIN	CLKOUT	CE
GTP_CLKBUFGMUX	CLKIN0,CLKIN1	CLKOUT	SEL
GTP_CLKBUFGMUX_E1	CLKIN0,CLKIN1	CLKOUT	SEL,EN
GTP_CLKBUFGMUX_E2	CLKIN0,CLKIN1	CLKOUT	SEL,DETECT_CLK0, DETECT_CLK1

The global clock GTP is mapped to USCM in the same way, and the interface is different. The following figure is the block diagram of GTP_CLKBUFG mapped to USCM:

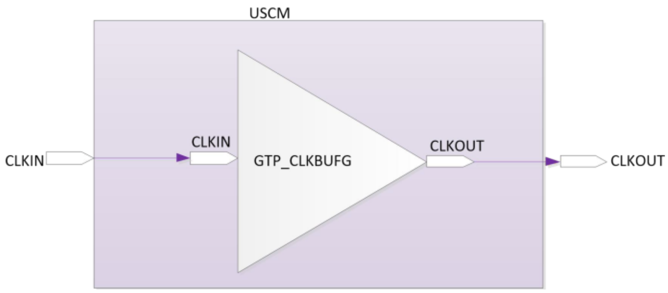


Figure 6 GTP_CLKBUFG Mapping to USCM SCHEMATIC

GTP_CLKBUFG

GTP_CLKBUFG provides a simple BUFG function, such as the clock coming in from the clock pin GSCLK/GMCLK directly drives the internal logic of the FPGA, and the software will automatically insert the USCM to let the clock go to the global clock network; you can manually instantiate the GTP_CLKBUFG primitive, which can constrain GTP_CLKBUFG to a USCM.

GTP_CLKBUFG primitive instantiation:

```
GTP_CLKBUFG GTP_CLKBUFG_INST (
.CLKOUT    (CLKOUT     ),
.CLKIN     (CLKIN      )
);
```

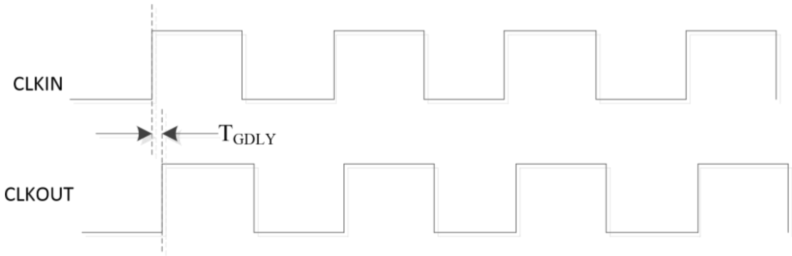


Figure 7 GTP_CLKBUFG port timing diagram

Note: TGDLY is the delay from input to output of USCM.

GTP_CLKBUFGCE

GTP_ CLKBUFGCE In addition to the GTP_CLKBUFG function, it also has the enable control port and parameter settings. When CE is low, the DEFAULT_VALUE parameter is set to 0, CLKOUT outputs low level, and the DEFAULT_VALUE parameter is set to 1, CLKOUT outputs high level; When CE is high, CLKOUT outputs the same frequency clock as CLKIN.

GTP_ CLKBUFGCE primitive instantiation:

```
GTP_CLKBUFGCE #(
.DEFAULT_VALUE (1'b0 ),
) GTP_CLKBUFGCE_INST (
.CLKOUT    (CLKOUT     ),
.CE        (CE         ),
.CLKIN     (CLKIN      )
);
```

Table 5 GTP_CLKBUFGCE port description

Port signal	Input/Output	Description
DEFAULT_VALUE	parameter	0/1; CLKOUT state when CE is not enabled
CLKIN	input	Input clock
CE	input	Clock enable, active high enable
CLKOUT	output	Output clock

The timing of the GTP_CLKBUFGCE port is shown in the figure below:

When the parameter DEFAULT_VALUE=1,

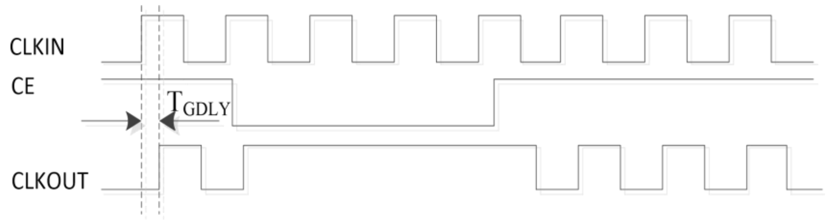
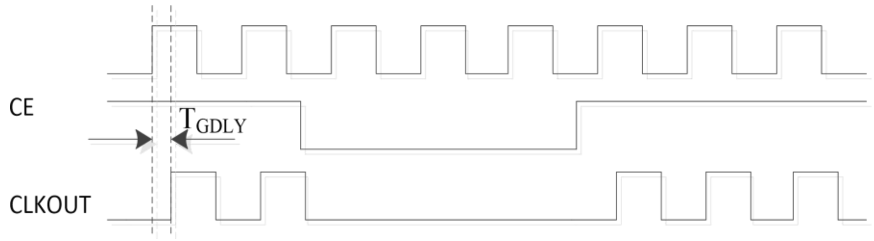


Figure 8 GTP_CLKBUFGCE port timing diagram 1

When the parameter DEFAULT_VALUE=0,

Figure 9 GTP_CLKBUFGCE port timing diagram 2



GTP_CLKBUFGMUX

GTP_CLKBUFGMUX has a selection control signal, which can realize dynamic switching between two clock sources. You can configure TRIGGER_MODE to select the switching mode according to the parameter, and switch the "NORMAL" mode asynchronously, which occurs at any time, and glitches may occur when switching; and The other two modes are synchronous switching, the glitchless switching triggered by the falling edge of the clock, and the glitchless switching triggered by the rising edge of the clock, which are switched only on the rising or falling edge of the clock, so glitches can be avoided. Clock edge switching mode switching The process needs to take 4 beats (the total number of beats of the two input clock edges), and the last two beats CLKOUT keeps high/low level unchanged, and cannot output a valid clock signal. When switching synchronously, it must be ensured that both clock sources are valid, and asynchronous switching cannot subject to this condition.

CLKBUFGMUX primitive instantiation:

```
GTP_CLKBUFGMUX #(
.TRIGGER_MODE  ("NORMAL"   ),
) GTP_CLKBUFGMUX_INST (
.CLKOUT    (CLKOUT     ),
.CLKIN0    (CLKIN0     ),
.CLKIN1    (CLKIN1     ),
.SEL       (SEL        )
);
```

Table 6 GTP_CLKBUFGMUX port description

Port Signal	input / Output	Description
CLKIN0	Input	Input clock 0
CLKIN1	Input	Input clock 1
SEL	Input	Clock selection signal, 0 selects CLK0; 1 selects CLK1;
CLKOUT	Output	Output clock

Table 7 GTP_CLKBUFGMUX parameter description

Parameter name	Parameter Type	Valid value	Defaults	Functional description
TRIGGER_MODE	<string>	"NORMAL" "NEGEDGE" "POSEDGE"	"NORMAL"	(1) "NORMAL": In this mode, the input clock (CLKIN0 and CLKIN1) can be freely switched without deburring function (2) "NEGEDGE": In this mode, the input clock (CLKIN0 and CLKIN1) can be switched freely, and the deburring function is provided by Clock falling edge trigger. (3) "POSEDGE": In this mode, the input clock (CLKIN0 and CLKIN1) can be switched freely, and the deburring function is provided by Clock rising edge trigger.

The timing diagram of the GTP_CLKBUFGMUX port is shown below. When clock switching is performed in the TRIGGER_MODE="NEGEDGE" and TRIGGER_MODE="POSEDGE" modes respectively, its level will maintain the current value until the next clock falling edge and rising edge respectively.

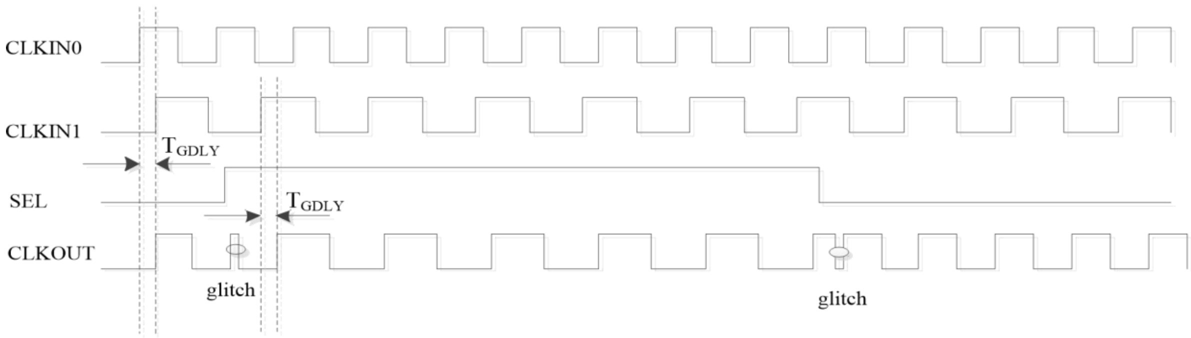


Figure 10 CLKBUFGMUX port timing diagram 1(TRIGGER_MODE="NORMAL")

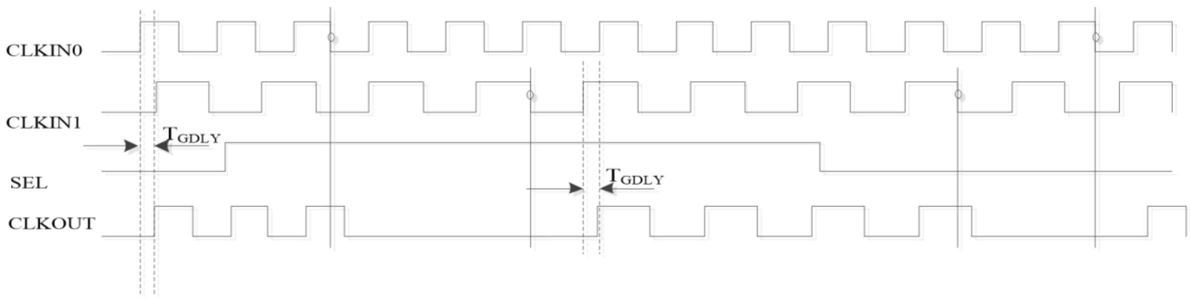


Figure 11 CLKBUFGMUX port timing diagram 2(TRIGGER_MODE=" NEGEDGE")

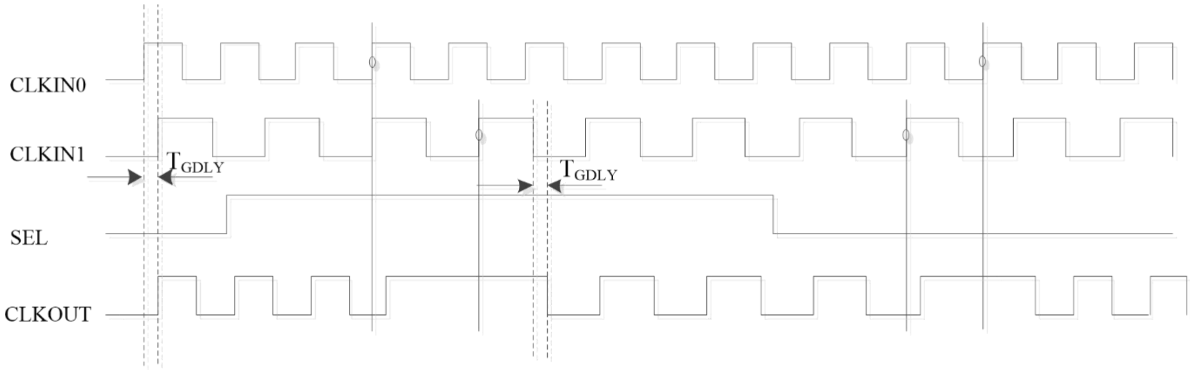


Figure 12 CLKBUFGMUX port timing diagram3(TRIGGER_MODE=" POSEDGE")

GTP_CLKBUFGMUX_E1

GTP_CLKBUFGMUX_E1 has some GTP functions of GTP_ CLKBUFGCE and GTP_CLKBUFGMUX. The EN signal is used to control whether CLKOUT outputs a clock signal, and the SEL signal is used to realize the function of dynamic switching of the input clock. Different from the parameter settings of GTP_CLKBUFGMUX, only two switching modes are supported. NEGEDGE "mode and "POSEDGE" mode, there is no device parameter setting, the parameter "INIT_SEL" can set the initial output clock.

GTP_CLKBUFGMUX_E1 primitive instantiation:

```
GTP_CLKBUFGMUX_E1 #(
.TRIGGER_MODE   ("NEGEDGE" ),
.INIT_SEL       ("CLK0"    )
) GTP_CLKBUFGMUX_E1_INST(
.CLKOUT    (CLKOUT     ),
.CLKIN0    (CLKIN0     ),
.CLKIN1    (CLKIN1     ),
.EN        (EN    ),
.SEL       (SEL   )
);
```

Table 8 GTP_CLKBUFGMUX_E1 port description

Port Signal	Input / Output	Description
CLKIN0	Input	input clock 0
CLKIN1	Input	input clock 1
EN	Input	Clock enable control signal: EN = 1, CLKOUT output clock signal. EN = 0, CLKOUT does not output clock signal.

Port Signal	Input / Output	Description
SEL	Input	Clock selection control signals: SEL = 1, select output CLKIN1. SEL = 0, select output CLKIN0.
CLKOUT	Output	Output clock

Table 9 GTP_CLKBUFGMUX_E1 parameter description

Parameter name	Parameter Type	Valid value	Defaults	Functional description
TRIGGER_MODE	<string>	"POSEDGE" or "NEGEDGE"	"NEGEDGE"	Select clock rising edge trigger or falling edge trigger: When it is set to "NEGEDGE", the falling edge trigger is used, and when it is set to "POSEDGE", the rising edge trigger is used.
INIT_SEL	<string>	"CLK0" or "CLK1"	"CLK0"	Select initial output clock: when set to "CLK0", CLKOUT = CLKIN0, when set to "CLK1", CLKOUT = CLKIN1.

GTP_CLKBUFGMUX_E1 port timing:

1. When TRIGGER_MODE = "NEGEDGE", INIT_SEL = "CLK0", falling edge trigger, when the initial clock selects CLKIN0, the port timing diagram is as follows:

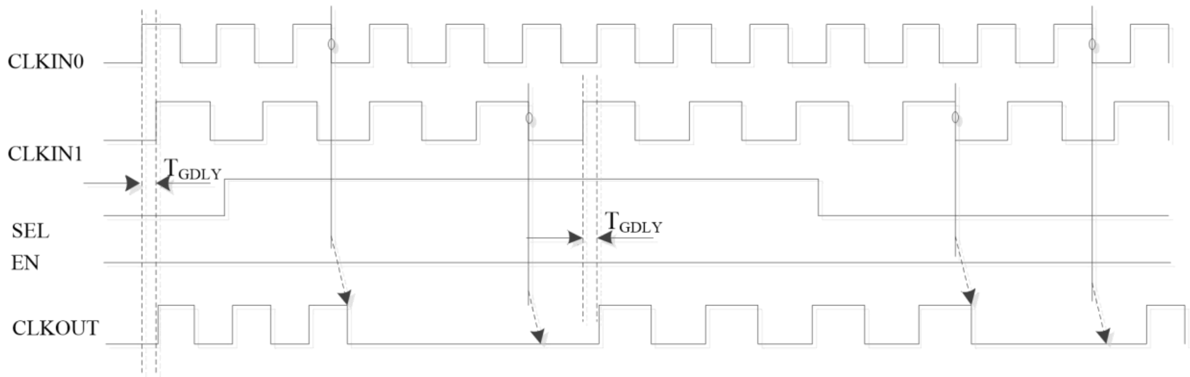


Figure 13 GTP_CLKBUFGMUX_E1 port timing diagram 1

1) EN = 1:

- When SEL changes from 0 to 1, it is necessary to detect the falling edge of the current clock CLKIN0 twice, and then detect the falling edge of the switched clock CLKIN1 twice (during the process of detecting the falling edge of the switched clock, CLKOUT outputs a low level). After the detection is completed, CLKOUT is switched from CLKIN0 to CLKIN1.
- Conversely, when SEL changes from 1 to 0, first detect the falling edge of CLKIN1 twice, and then detect the falling edge of CLKIN0 twice (during the process of detecting the falling edge of the switched clock CLKIN0, CLKOUT outputs low level). After the detection is completed CLKOUT is switched from CLKIN1 to CLKIN0.

2) When EN = 0, the SEL signal is not allowed to jump, and after detecting the falling edge of CLKOUT twice, output a low level.

2. When TRIGGER_MODE = "POSEDGE", INIT_SEL = "CLK0", the rising edge is triggered, and the port timing is as follows when the initial clock is CLKIN0:

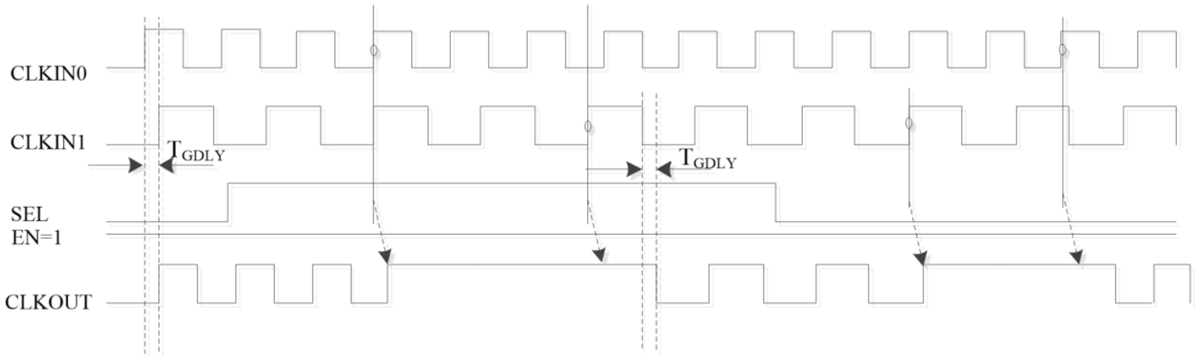


Figure 14 GTP_CLKBUFGMUX_E1 port timing diagram2

1) When EN = 1:

- When SEL changes from 0 to 1, it is necessary to detect the rising edge of the current clock CLKIN0 twice, and then detect the rising edge of the switched clock CLKIN1 twice (during the detection of the rising edge of the switched clock, CLKOUT outputs a high level). Detection CLKOUT switches from CLKIN0 to CLKIN1 after completion.
- Conversely, when SEL changes from 1 to 0, first detect the rising edge of CLKIN1 twice, and then detect the rising edge of CLKIN0 twice (during the process of detecting the rising edge of the switched clock CLKIN0, CLKOUT outputs high level). After the detection is completed CLKOUT is switched from CLKIN1 to CLKIN0.

2) When EN = 0, the SEL signal is not allowed to jump. And after detecting the rising edge of CLKOUT twice, output a high level.

When INIT_SEL = "CLK1", the default input clock is CLKIN1, and the switching timing diagram follows the above two methods. The default value of CLKOUT changes from CLKIN0 to CLKIN1, and there is no difference in other.

Note: The dotted arrow points to the clock switching time

3. Only one clock source is valid

When EN=1 and only one clock source is valid, it is necessary to ensure that the INIT_SEL parameter setting is consistent with the valid clock source 1:

- CLKIN0 is valid, CLKIN1=1/0,INIT_SEL="CLK0",SEL=0,CLKOUT=CLKIN0.
- CLKIN0 is valid, CLKIN1=1/0,INIT_SEL="CLK0",SEL=1,CLKOUT=0/1.
- CLKIN0=1/0,CLKIN1 is valid, INIT_SEL="CLK1",SEL=0,CLKOUT=0/1.
- CLKIN0=1/0,CLKIN1 is valid, INIT_SEL="CLK1",SEL=1,CLKOUT= CLKIN1.

TRIGGER_MODE is set to "POSEDGE", the value is 1 when the CLKOUT output remains unchanged, and it is set to "NEGEDGE", the value is 0 when the CLKOUT output remains unchanged.

GTP_CLKBUFGMUX_E2

GTP_CLKBUFGMUX_E2 also has the function of dynamic switching of input clocks, and has some functional

characteristics of GTP_CLKBUFGMUX and GTP_CLKBUFGMUX_E1. The biggest difference from these two GTPs is that this GTP can choose which input clock edge detection to switch (two clock edges, one clock edge , and neither clock edge is detected); when only one of the input clock edges is detected, the SEL signal can be regarded as an enable signal, for example, when DETECT_CLK0=1, DETECT_CLK1=0, SEL is 0 output The clock is consistent with CLKIN0 1, SEL is 1, the output clock remains 1/0 unchanged, when DETECT_CLK0=0, DETECT_CLK1=1, SEL is 0, the output clock remains 1/0 unchanged, SEL is 1, the output clock is consistent with CLKIN1 1. It also has parameter settings for initial output clock (CLKIN0 or CLKIN1) and clock source trigger mode (rising edge or falling edge). Select these 3 GTP according to actual application requirements.

The following points to note:

- The two input clock edges are not detected, and there will be glitches when the input clock switches;
- If you set both input clock edges to be detected at the beginning, and only one of them is used to detect midway, glitches may also occur when DETECT_CLK0 and DETECT_CLK0=1 jump from 1 to 0. For details, see the second and third points of the interface timing description ;
- Dual clock edge detection switching needs to wait for 4 beats, single clock edge detection switching needs to wait for 2 beats, and switch immediately without detection, see the interface timing description for details.

GTP_CLKBUFGMUX_E2 primitive instantiation:

```
GTP_CLKBUFGMUX_E2 #(
.TRIGGER_MODE ("NEGEDGE"  ),
.INIT_SEL ("CLK0"     )
) GTP_CLKBUFGMUX_E2_INST (

.CLKOUT         (CLKOUT          ),
.CLKIN0         (CLKIN0          ),
.CLKIN1         (CLKIN1          ),
.DETECT_CLK0    (DETECT_CLK0     ),
.DETECT_CLK1    (DETECT_CLK1     ),
.SEL            (SEL             )
);
```

Table 10 GTP_CLKBUFGMUX_E2 port description

Port Signal	Input / Output	Description
CLKIN0	Input	Input clock 0
CLKIN1	Input	Input clock 1

Port Signal	Input / Output	Description
DETECT_CLK0	Input	When set to 1: During clock switching, detect the clock edge of CLKIN0. When set to 0: In the process of switching the clock, do not detect the clock edge of CLKIN0.
DETECT_CLK1	Input	When set to 1: During clock switching, detect the clock edge of CLKIN1. When set to 0: In the process of switching clock, do not detect the clock edge of CLKIN1.
SEL	Input	Clock Select Control Signal SEL = 1, select CLKIN1 SEL = 0, select CLKIN0
CLKOUT	Output	Output clock

Table 11 GTP_CLKBUFGMUX_E2 parameter description

Parameter name	Parameter Type	Valid value	Defaults	Functional description
TRIGGER_MODE	<string>	"POSEDGE" or "NEGEDGE"	"NEGEDGE"	Select clock rising edge trigger or falling edge trigger: When it is set to "NEGEDGE", the falling edge trigger is used, When it is set to "POSEDGE", the rising edge trigger is used.
INIT_SEL	<string>	"CLK0" or "CLK1"	"CLK0"	Select initial output clock: When set to "CLK0", CLKOUT = CLKIN0, When set to "CLK1", CLKOUT = CLKIN1.

The CLKOUT output of DETECT_CLK0, DETECT_CLK1, SEL and TRIGGER_MODE are shown in Table 12. In the table, CLKIN0 is valid. When CLKIN1=1/0, the INIT_SEL parameter is set to "CLK0". When CLKIN0=1/0, CLKIN1 is valid, the INIT_SEL parameter is set It is "CLK1". When only one clock source is valid, it is necessary to ensure that the INIT_SEL parameter setting is consistent with the valid clock source 1.

Table 12 CLKOUT output results under different configurations of GTP_CLKBUFGMUX_E2

CLKIN0	CLKIN1	DETECT_CLK0	DETECT_CLK1	SEL	CLKOUT
Valid	Valid	0	0	0	CLKOUT=CLKIN0
		0	0	1	CLKOUT=CLKIN1
		1	0	0	CLKOUT=CLKIN0
		1	0	1	"NEGEDGE":0 "POSEDGE":1
		0	1	0	"NEGEDGE":0 "POSEDGE":1
		0	1	1	CLKOUT=CLKIN1
		1	1	0	CLKOUT=CLKIN0
		1	1	1	CLKOUT=CLKIN1

CLKIN0	CLKIN1	DETECT_CLK0	DETECT_CLK1	SEL	CLKOUT
Valid	1/0	0	0	0	CLKOUT=CLKIN0
		0	0	1	0
		1	0	0	CLKOUT=CLKIN0
		1	0	1	"NEGEDGE":0 "POSEDGE":1
		0	1	0	"NEGEDGE":0 "POSEDGE":1
		0	1	1	"NEGEDGE":0 "POSEDGE":1
		1	1	0	CLKOUT=CLKIN0
		1	1	1	"NEGEDGE":0 "POSEDGE":1
1/0	Valid	0	0	0	0
		0	0	1	CLKOUT=CLKIN1
		1	0	0	"NEGEDGE":0 "POSEDGE":1
		1	0	1	"NEGEDGE":0 "POSEDGE":1
		0	1	0	"NEGEDGE":0 "POSEDGE":1
		0	1	1	CLKOUT=CLKIN1
		1	1	0	"NEGEDGE":0 "POSEDGE":1
		1	1	1	CLKOUT=CLKIN1

GTP_CLKBUFGMUX_E2 port timing:

CLKOUT_NEG and CLKOUT_POS in the following 4 pictures refer to the CLKOUT output when the parameter TRIGGER_MODE is set to "NEGEDGE" and "POSEDGE" respectively. This setting is for the convenience of comparison, not to say that this GTP has 2 clock output terminals. 1 GTP only has 1 Output CLKOUT.

1. When DETECT_CLK0 = 1 and DETECT_CLK1 = 1, the detection of the two clock edges is not ignored. The initial clock of CLKOUT_NEG is CLKIN0, and the port timing is shown in the following figure:

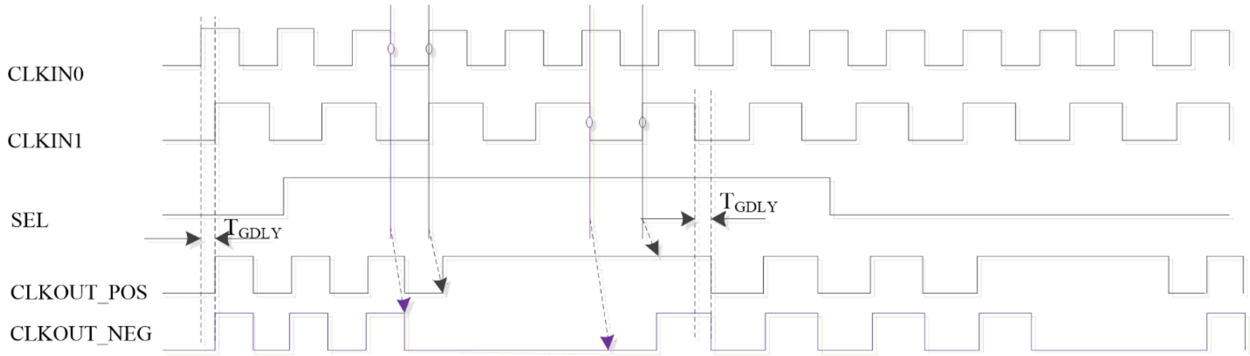


Figure 15 GTP_CLKBUFGMUX_E2 port timing diagram1

Take CLKOUT_NEG as an example:

1) When SEL changes from 0 to 1, it is necessary to detect the falling edge of the current clock CLKIN0 twice, and then detect the falling edge of the switched clock CLKIN1 twice (during the period of detecting the falling edge of CLKIN1 twice, CLKOUT_NEG outputs a low level). After the detection is completed, CLKOUT_NEG is switched from CLKIN0 to CLKIN1.

2) When SEL changes from 1 to 0, it is necessary to detect the falling edge of the current clock CLKIN1 twice, and then detect the falling edge of the switched clock CLKIN0 twice (during the period of detecting the falling edge of CLKIN0 twice, CLKOUT_NEG outputs a low level). After the detection is completed, CLKOUT_NEG is switched from CLKIN1 to CLKIN0.

The CLKOUT_POS switching process is similar to CLKOUT_NEG, except that the detection of the falling edge is replaced by the detection of the rising edge. When the rising edge of the switched clock is detected, the CLKOUT_POS switching process will output a high level after two beats.

2. When DETECT_CLK0 = 1 and DETECT_CLK1 = 0, detect the clock edge change of CLKIN0 and ignore the clock edge detection of CLKIN1. The port timing is shown in the following figure:

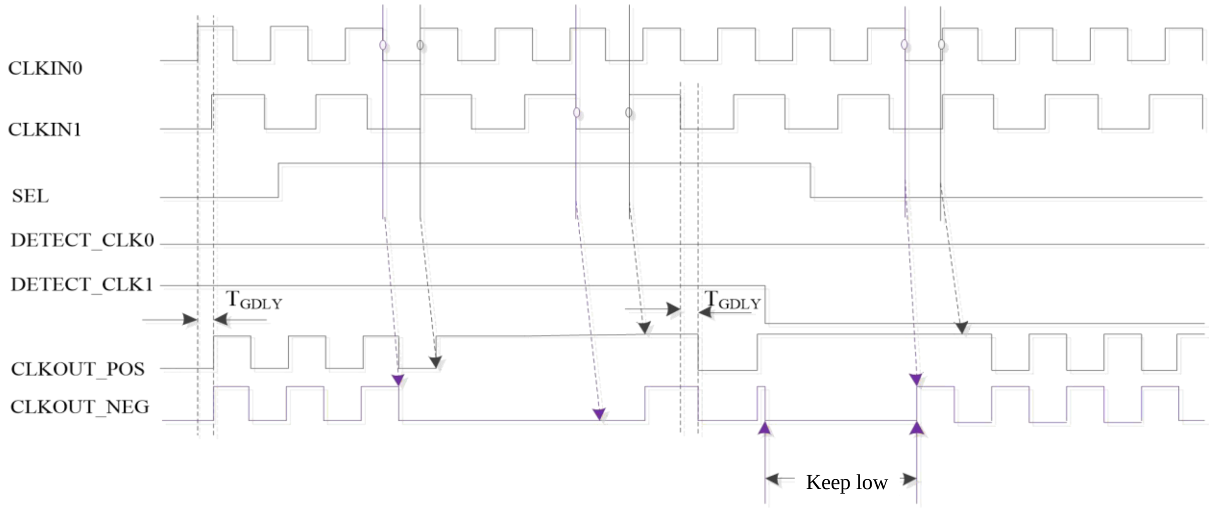


Figure 16 GTP_CLKBUFGMUX_E2 port timing diagram2

Take CLKOUT_NEG as an example, the initial clock is CLKIN0

1) When DETECT_CLK1 = 0 is set, CLKOUT_NEG no longer outputs CLKIN1, but outputs low level. At this time, when SEL changes from 1 to 0, the clock edge of CLKIN1 is no longer detected, and the falling edge of CLKIN0 is directly detected twice (CLKOUT_NEG outputs a low level during the detection of

the falling edge of CLKIN0). After the detection is completed, CLKOUT_NEG switches to CLKIN0.

2) The switching process of CLKOUT_POS is similar to CLKOUT_NEG, except that the detection of the falling edge is replaced by the detection of the rising edge. When the rising edge of the switched clock is detected, CLKOUT_POS outputs a high level.

3. When DETECT_CLK0 = 0 and DETECT_CLK1 = 1, ignore the clock edge change of CLKIN0 and detect the clock edge change of CLKIN1. The port timing is as follows:

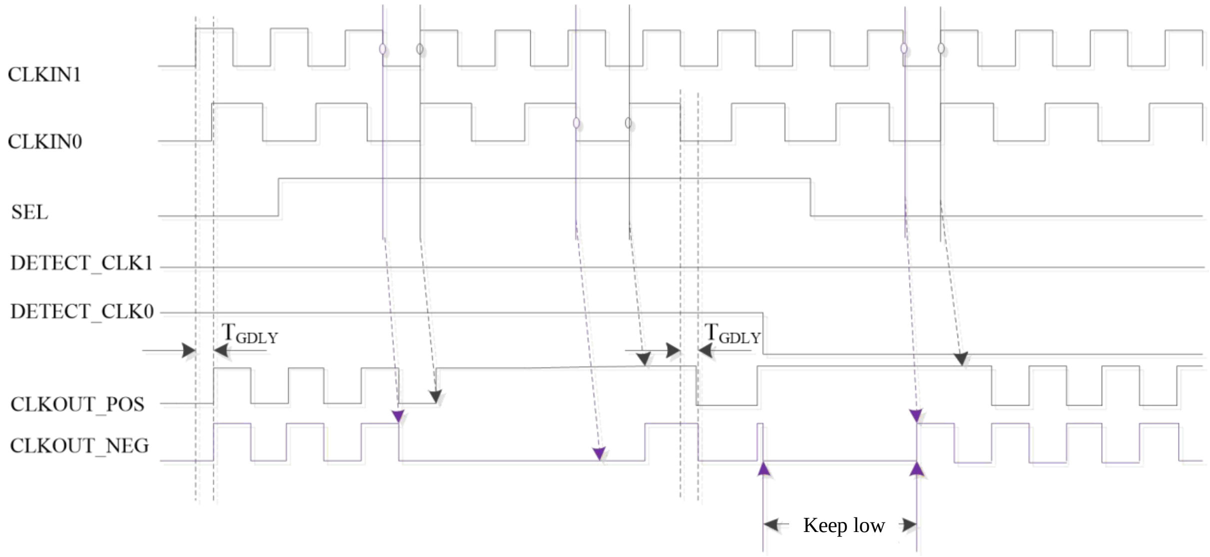


Figure 17 GTP_CLKBUFGMUX_E2 port timing diagram3

Take CLKOUT_NEG as an example, the initial clock is CLKIN1:

1) When DETECT_CLK0 = 0 is set, CLKOUT_NEG no longer outputs CLKIN0, but outputs low level. At this time, when SEL changes from 0 to 1, the clock edge of CLKIN0 is no longer detected, and the falling edge of CLKIN1 is directly detected twice (CLKOUT_NEG outputs a low level during the detection of the falling edge of CLKIN1). After the detection is completed, CLKOUT_NEG switches to CLKIN1.

2) The switching process of CLKOUT_POS is similar to CLKOUT_NEG, except that the detection of the falling edge is replaced by the detection of the rising edge. When the rising edge of the switched clock is detected, CLKOUT_POS outputs a high level.

4. When DETECT_CLK0 = 0, DETECT_CLK1 = 0

In this case, the clock edge detection of CLKIN0 and CLKIN1 is ignored, and the clock edge change of the current clock and the switched clock is not detected when the clock is switched, but when SEL changes, CLKOUT_NEG and CLKOUT_POS switch the clock immediately. In this mode , the output clock may have glitches, and the interface timing is shown in the figure below:

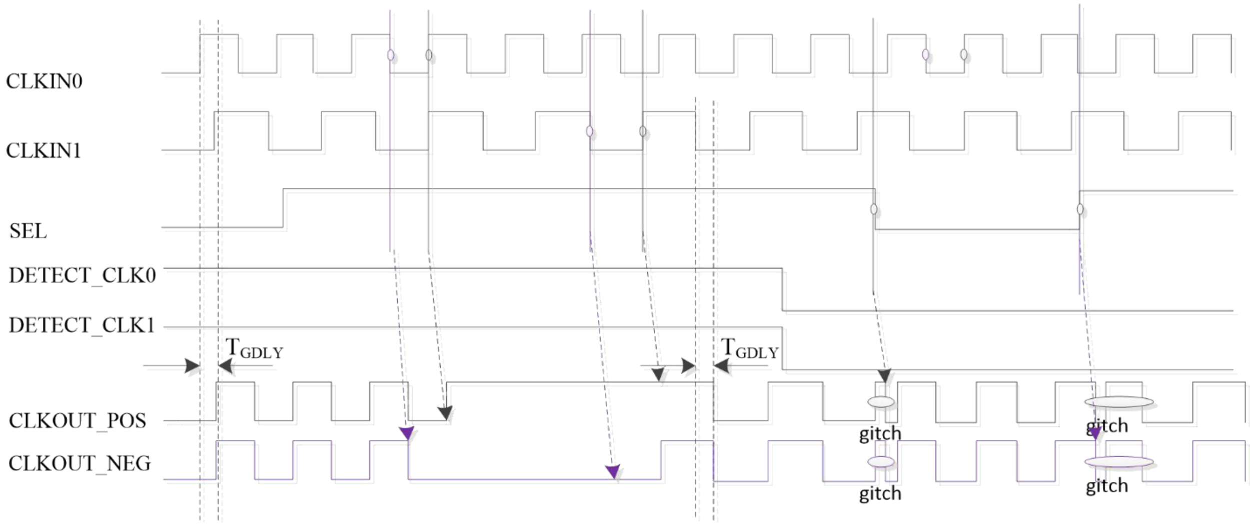


Figure 18 GTP_CLKBUFGMUX_E2 port timing diagram4

Note: The dotted arrow points to the clock switching time

3. Horizontal clock resource

3.1 Horizontal clock network

The horizontal clock (HCKB) mainly provides synchronous clocks for the logic units of the two REGIONs in the horizontal direction. Each HCKB has an independent synchronization enable control signal, and each REGION has 12 HCKBs.

The input sources of HCKB are:

- Clock input pins GSCLK, GMCLK of the same or adjacent horizontal areas.
- PPLL/GPLL output clocks in the same or adjacent horizontal areas.
- HSSTHP output clocks for the same or adjacent horizontal regions
- SRB (not recommended).
- USCM.

The horizontal clock can be driven by:

- GPLL/PPLL in the same area.
- Any logic unit with a clock pin.
- IOLs in the same area
- USCMs in the same half area
- HSSTHP's 4 RX user clocks, 4 TX user clocks and 2 reference clocks (see "UG050008_Titan2" for details).

GPLL output clocks include: CLKFBOUTN, CLKOUTN0N~3N, CLKFBOUT, CLKOUT0~6.

PPLL output clocks include: CLKOUT0N, CLKFBOUT, CLKFBOUTN, CLKOUT0~4.

HCKB has a synchronous dynamic enable function. According to Figure 1, the connection relationship of the clock input sources of the HCKB in adjacent horizontal areas with symmetrical clock resources is consistent with Figure 19 1; The connection relationship of the input sources is consistent with Figure 20 1. In the figure, the HCKB can only reach the USCM in the same upper or lower half area, and the HCKB output in the area where the HSSTHP is located cannot be used as the USCM clock source, while the outputs of all USCMs can reach all of the chips. For HCKB, in order to ensure the quality of the clock signal, it is not recommended to use the SRB clock.

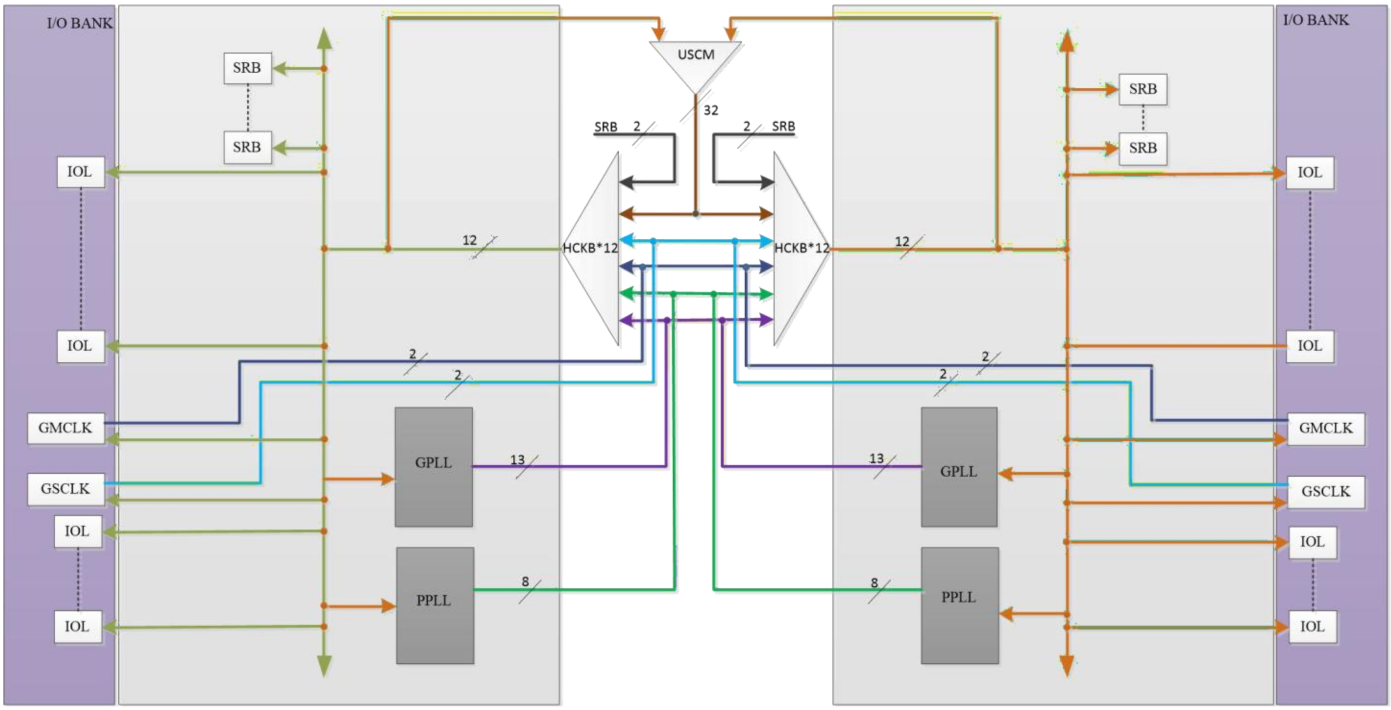


Figure 19 No HSSTHP Region Horizontal Clock Adjacent Region HCKB Input Clock Source and Output Connection Diagrams

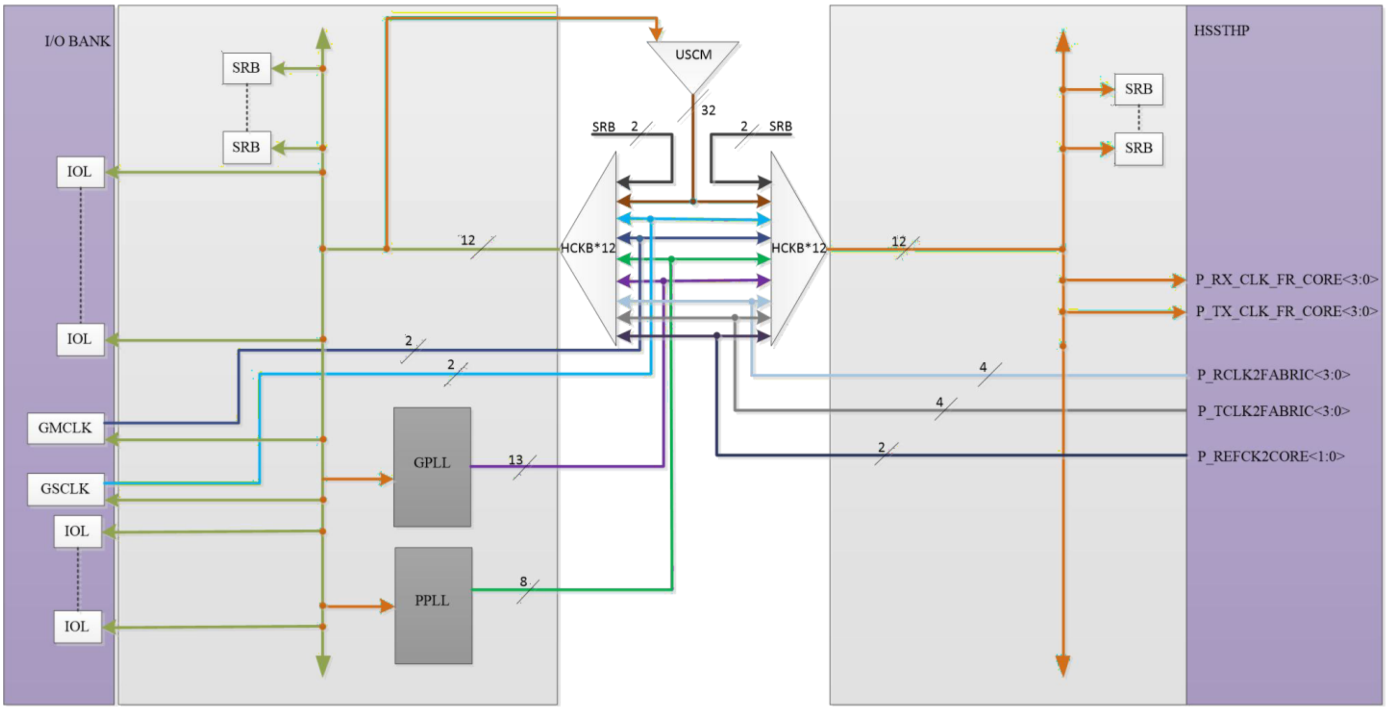


Figure 20 Schematic diagram of HCKB input clock source and output connections for horizontal adjacent areas with HSSTHP areas

The output clock of HCKB drives the GPLL/PPLL, HSSTHP clock, SRB, and IOL in the same area, as shown in Figure 19 and Figure 20. Since HSSTHP occupies more clock resources, when using it, give priority to horizontal clock resources.

The HSST CLK of each HSSTHP includes 4 RX-side user clocks, 4 TX-side user clocks and two reference clocks.

3.2 Horizontal Clock GTP

One horizontal clock GTP occupies 1 HCKB, and each area supports up to 12 at the same time.Titan2 series products have two horizontal clock GTPs, one is GTP_CLKBUFX with only input and output; the other is GTP_CLKBUFXCE with enable control signal , through the enable signal CE to control whether to output the clock signal, the power consumption can be reduced.

If the design module is only in one region or adjacent horizontal regions, the input clock does not need to go through the global clock tree. By manually instantiating the horizontal clock GTP, the input clock can directly go through the HCKB to drive the logic of the module. At the same time, the user can also according to Self-design needs to constrain the instantiated primitives to the desired position to achieve the design purpose.

GTP_CLKBUFX

GTP_CLKBUFX has no parameters, only one input and output, and the output clock frequency is equal to the input clock frequency.

GTP_CLKBUFX primitive instantiation:

```
GTP_CLKBUFX    GTP_CLKBUFX_INST
(
.CLKIN     (CLKIN      ),
.CLKOUT    (CLKOUT     )
);
```

The timing of the GTP_CLKBUFX port is shown in the figure below:

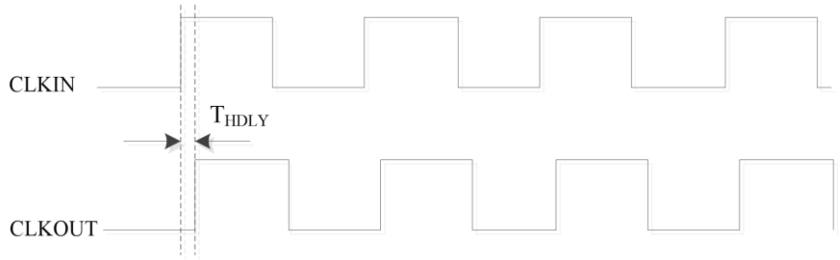


Figure 21 GTP_CLKBUFX port timing diagram

Note: THDLY is the delay time from input to output of HCKB

GTP_CLKBUFXCE

GTP_CLKBUFXCE has the enable control signal CE, which controls whether to output the clock signal. By changing the parameters, you can set the enable mode (synchronous enable or asynchronous enable), enable active level (active high or active low), and Trigger mode (rising edge trigger or falling edge trigger). It should be noted that in the case of asynchronous enable, the output clock will be pulled down or pulled up immediately when the enable signal CE changes from high to low, and glitches may occur during switching. In the case of synchronous enable, each switch needs to wait for 2 clock edges It will be switched, and the rising edge or falling edge is determined by the trigger mode.

GTP_CLKBUFXCE primitive instantiation:

```
GTP_CLKBUFXCE #(
.CE_TYPE  ("SYNC"    ),
.CE_INV   ("FALSE"   ),
.TRIGGER_MODE ("POSEDGE")
) GTP_CLKBUFXCE_INST (
.CLKOUT   (CLKOUT    ),
.CE       (CE        ),
.CLKIN    (CLKIN     )
);
```

Table 13 GTP_CLKBUFXCE port description

CLKIN0	Input	Input clock 0
CLKIN	Input	Input clock signal
CE	Input	Clock enable terminal
CLKOUT	Output	Output clock signal

Table 14 GTP_CLKBUFXCE parameter description

Parameter name	Parameter Type	Valid value	Defaults	Functional description
CE_TYPE	<string>	"SYNC"/"ASYNC"	"SYNC"	CE_TYPE= "SYNC", support synchronous enable. CE_TYPE= "ASYNC", support asynchronous enable.
TRIGGER_MODE	<string>	"POSEDGE"/"NEGEDGE"	"POSEDGE"	TRIGGER_MODE = "POSEDGE", Support clock output initial value equal to 1’b1, rising edge trigger. TRIGGER_MODE="NEGEDGE", Support clock output initial value equal to 1’b0, falling edge trigger.
CE_INV	<string>	"TRUE" /"FALSE"	"FALSE"	EN_INV= "FALSE", the default CE is active high. EN_INV="TRUE", CE is active low by default.

1. Synchronous enable mode

When configured as rising edge trigger synchronization enable, the output clock is triggered by the rising edge of the input clock, and the output clock remains high when the enable is invalid; when configured as falling edge trigger synchronization enable, the output clock is triggered by the input clock The falling edge of the clock is triggered, and the output clock remains low when the enable is invalid. The port timing is shown in the following figure:

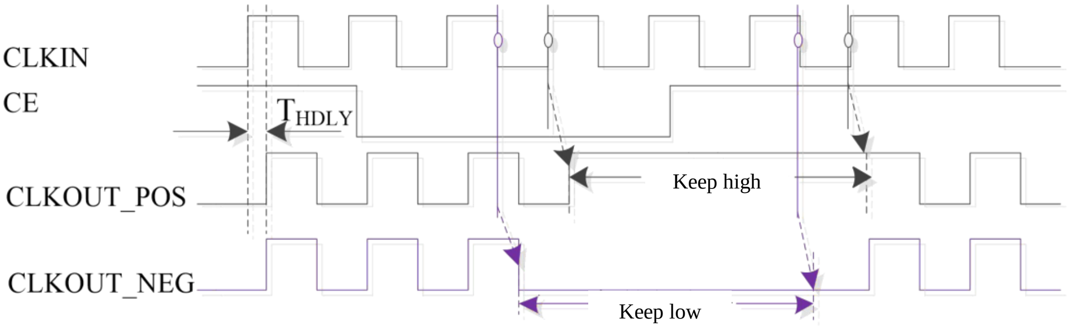


Figure 22 GTP_CLKBUFXCE port timing diagram 1

CLKOUT_POS represents the output clock when TRIGGER_MODE = "POSEDGE", CLKOUT_NEG represents the output clock when TRIGGER_MODE = "NEGEDGE", the dotted arrow indicates the clock switching time, and the default level of CE is low.

2. Asynchronous enable mode

When configured as asynchronous enable, the output clock switches immediately when the enable signal CE switches. In this case, glitches may occur. The port timing is shown in the following figure:

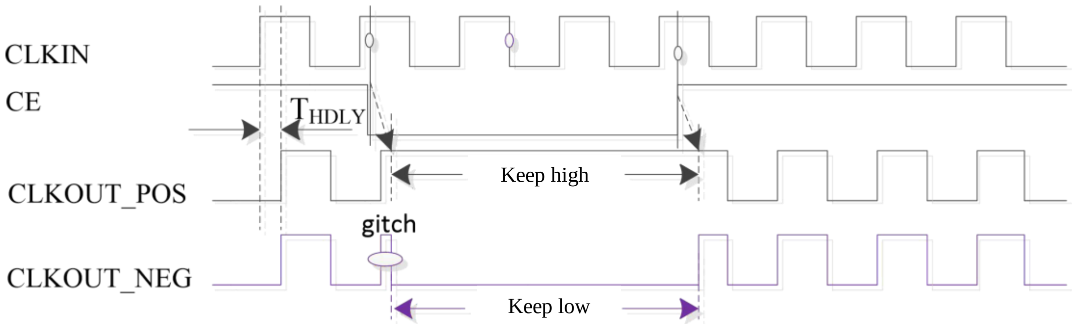


Figure 23 GTP_CLKBUFXCE port timing diagram2

CLKOUT_POS represents the output clock when TRIGGER_MODE = "POSEDGE", CLKOUT_NEG represents the output clock when TRIGGER_MODE = "NEGEDGE", the dotted arrow indicates the clock switching time, and the default level of CE is low.

4. Regional clock resources

4.1 Regional clock network

REGIONAL CLK is based on Region distribution, and each Region has 4 REGIONAL CLK networks. The regional clock mainly provides a synchronous clock for the logic unit of a single REGION, driven by RCKB.

Figure 24 is a schematic diagram of the scope of RCKB in a single area of the chip. Since there are no RCKB and MRCKB in the area where HSSTHP is located, the input and output connections of RCKB in other areas are consistent with this figure except for the area where HSSTHP is located.

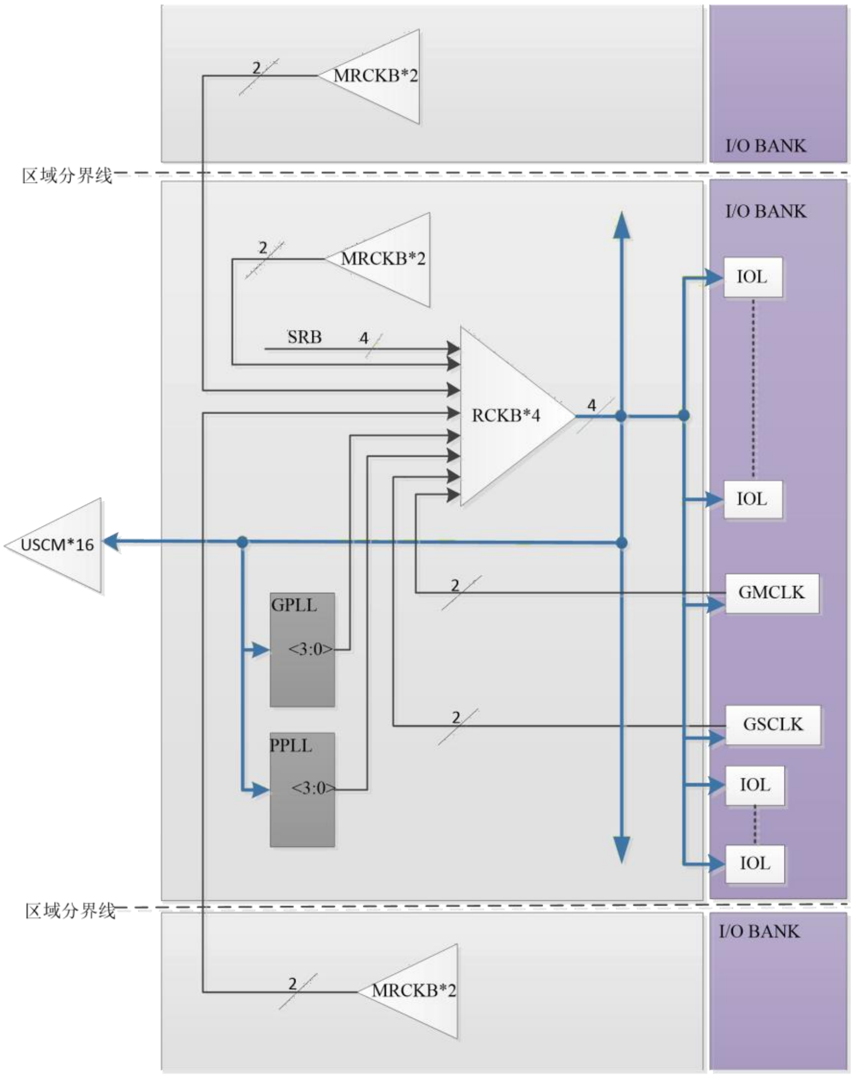


Figure 24 Regional Clock Input Clock Resource and Output Connection Diagrams

The input sources of RCKB are:

- Clock input pins GSCLK and GMCLK in the same region.
- PPLL and GPLL output clock CLKOUT0~3/N in the same region.
- The MRCKB of this area and two vertically adjacent areas.
- SRB.

RCKB can drive:

- GPLL/PPLL in the same area.
- Any logic unit with a clock pin.
- IOLs in the same area.
- USCM of the same half area (upper\lower).
- SRB

4.2 Regional clock GTP

A regional clock GTP occupies one RCKB, and a maximum of 4 can be used in the same region. If the design module is only in one region, the user can manually insert the regional clock GTP so that the clock does not go through the global clock network and directly drives logic resources through the RCKB.

Titan2 series products have two kinds of regional clock GTP, one is GTP_CLKBUFR with only input and output; the other is GTP_IOCLKDIV_E2 with frequency division function, by controlling DIV_FACTOR, it can realize frequency division from 1 to 8 and pass-through mode (BYPASS), At the same time, the GTP has a reset function and an enable control signal, through which the enable terminal CE can control whether to output the clock signal.

GTP_IOCLKDIV_E2 can be used in conjunction with GTP_CLKBUFM/GTP_CLKBUFMCE and GTP_IOCLKBUF to drive IOL across vertically adjacent regions, as a low-speed clock terminal for ISERDES/OSERDES, and can also drive internal logic.

GTP_CLKBUFR

GTP_CLKBUFR has no parameters, only one input and output, and the output clock frequency is equal to the input clock frequency.

GTP_CLKBUFR primitive instantiation:

```
GTP_CLKBUFR     GTP_CLKBUFR_INST
(
.CLKIN     (CLKIN      ),
.CLKOUT    (CLKOUT     )
);
```

The timing of the GTP_CLKBUFR port is shown in the figure below:

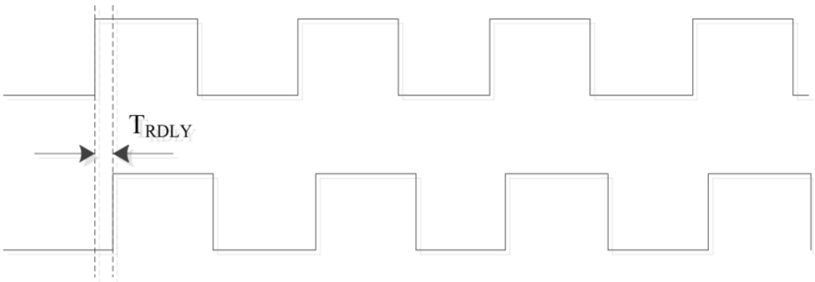


Figure 25 GTP_CLKBUFR port timing diagram

Note: TRDLY is the delay time from input to output of RCKB

GTP_IOCLKDIV_E2

GTP_IOCLKDIV_E2 has 3 input terminals CLKIN, RST_N, CE and 1 output terminal CLKDIVOUT and 1 parameter DIV_FACTOR. By controlling DIV_FACTOR, it can realize 1 to 8 frequency division and direct mode (BYPASS).

- CE is an asynchronous enable control. When CE = 0, CLKDIVOUT maintains the current level; when CE = 1, CLKDIVOUT outputs effective frequency division.

- RST_N is a reset signal that supports asynchronous reset and synchronous release. When RST_N = 0, the output clock is cleared.
- BYPASS mode is not affected by CE or RST_N.

GTP_IOCLKDIV_E2 primitive instantiation:

```
GTP_IOCLKDIV_E2 #(
.DIV_FACTOR     ("BYPASS"  )
) IOCLKDIV_E2_INST (
.CLKDIVOUT(CLKDIVOUT ),
.CE        (CE         ),
.CLKIN     (CLKIN      ),
.RST_N     (RST_N      )
);
```

Table 15 GTP_IOCLKDIV_E2 port description

CLKIN0	Input	Input clock 0
CLKIN	Input	Input clock
RST_N	Input	Reset signal, active low
CE	Input	Enable control: CE = 1, the output clock signal after frequency division or no frequency division CE = 0, the output clock maintains the current level
CLKDIVOUT	Output	Output clock

Table 16 GTP_CLKBUFXCE parameter description

Parameter name	Parameter Type	Valid value	Defaults	Functional description
DIV_FACTOR	<string>	"BYPASS" "1~8"	"BYPASS"	Mode selection, including direct mode and 1~8 frequency division mode

Taking the output clock divided by 1 and divided by 2 as an example, the port timing is shown in the figure below:

When RST_N is low level, CLKOUT output is 0, when RST_N and CE are high level, CLKOUT outputs a valid clock, when CE is low level, CLKOUT is pulled low immediately, and the output is 0.

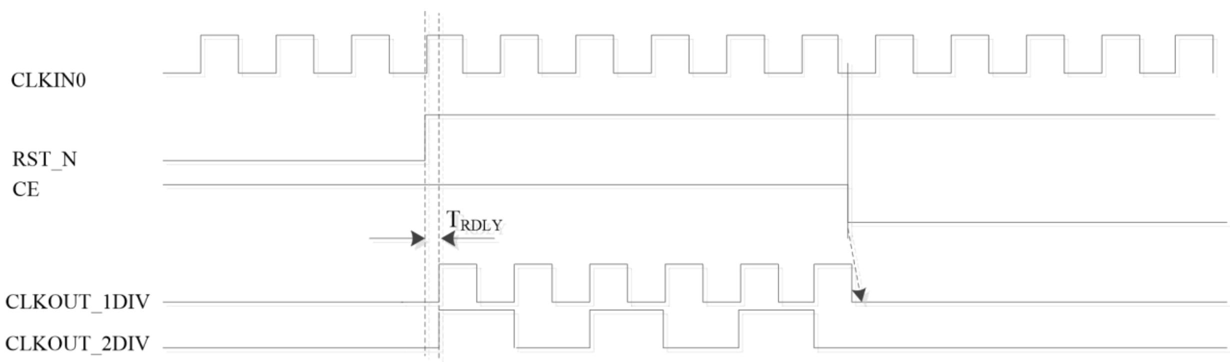


Figure 26 GTP_IOCLKDIV_E2 port timing diagram

5. IO clock resources

5.1 IO clock network

IO CLK provides a high-speed clock for the IO of Titan2 series products. It is often used in high-speed interface logic and is driven by IOCKB. Compared with GCLK/RCLK, IO CLK has the characteristics of high frequency, short delay time, and small skew.

PG2T390H has 4 IOCKBs driving the IO CLK clock line in each clock region, as shown in the figure below.

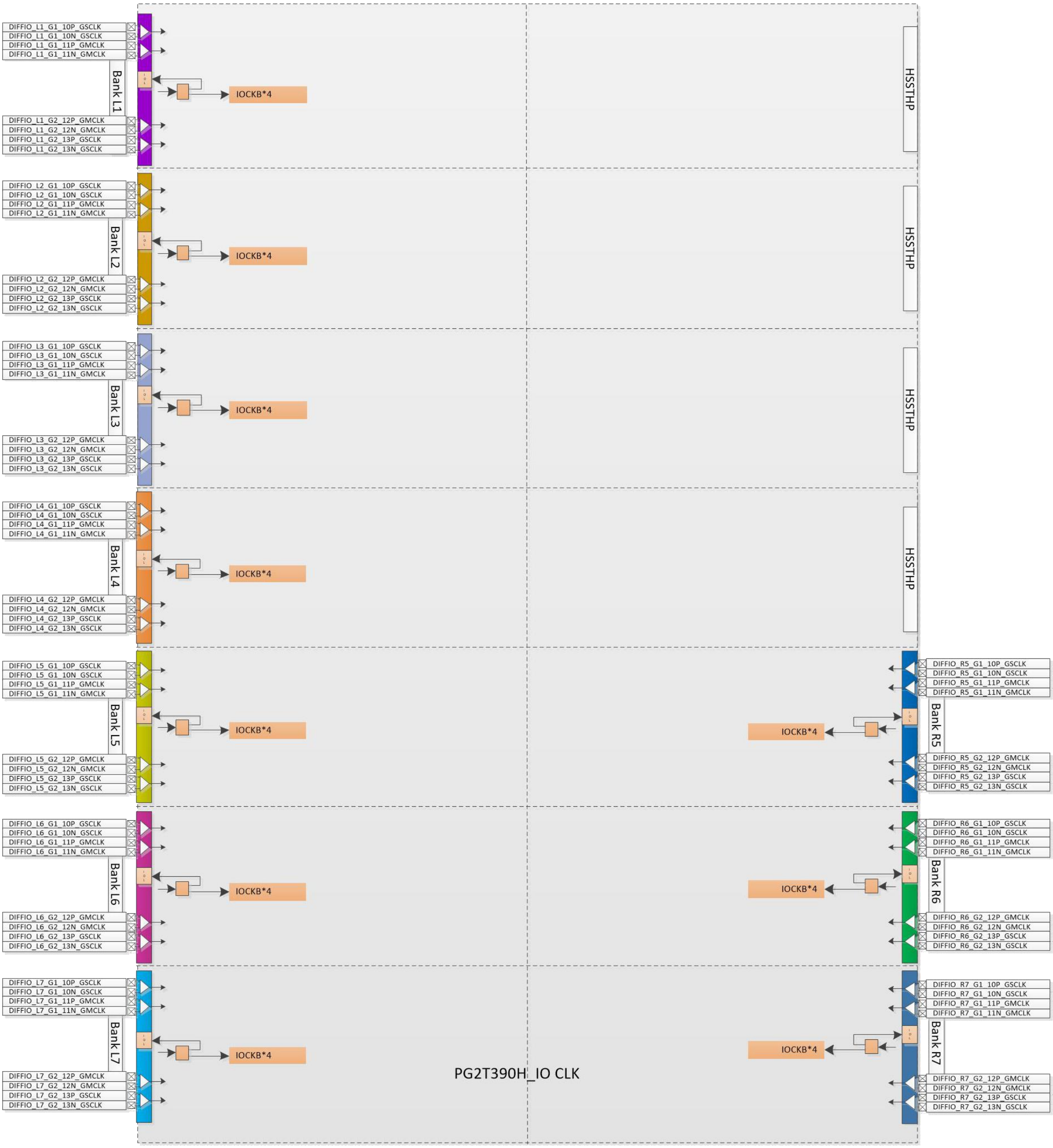


Figure 27 IO CLK clock resource schematic

As shown in the figure below, the output clock CLKOUT3~0 of GPLL and PPLL provides high-quality high-speed clock for IOL in BANK through IOCKB.

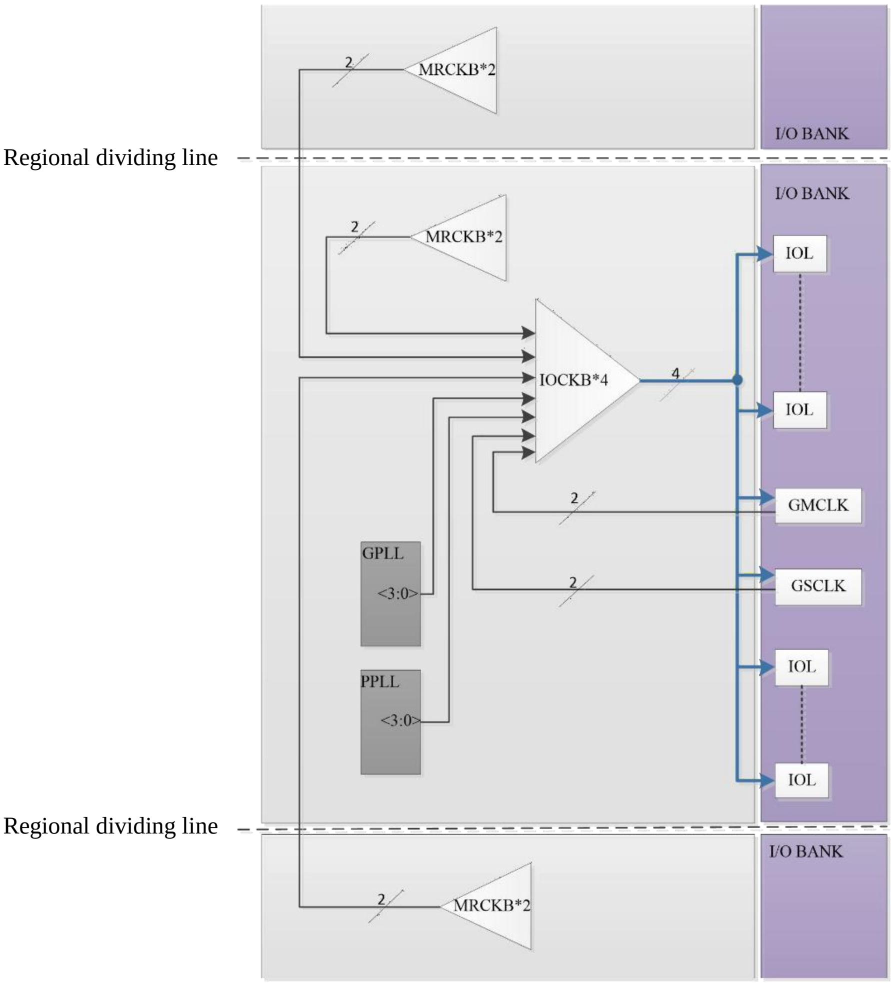


Figure 28 IO clock input clock source and output connection diagram

The figure above is a schematic diagram of IOCKB in a single area. The diagram clearly defines the input clock source and output drive range of IOCKB. Since there are no IOCKB and MRCKB in the area where HSSTHP is located, the IOCKB input and output connections in other areas are consistent with the figure except for the area where HSSTHP is located.

IOCKB input sources are:

- Clock input pins GSCLK and GMCLK in the same region.
- PPLL and GPLL output clock CLKOUT0~3/N in the same region.
- MRCKB in the same area and vertically adjacent BANK.

IOCKB can drive IOL in the same area.

5.2 IO clock GTP

An IO clock GTP occupies 1 IOCKB, and supports up to 4 in the same area at the same time. The IO clock can only drive the IOL in the same area, and is usually used as the input of the ISERDES/OSERDES high-speed clock interface.

GTP_IOCLKBUF primitive instantiation:

```
GTP_IOCLKBUF #(
.GATE_EN  ("FALSE"    )
) GTP_IOCLKBUF_INST (
.CLKIN    (CLKIN      ),
.DI       (DI         ),
.CLKOUT   (CLKOUT     )
);
```

Table 17 GTP_IOCLKBUF port description

Port Signal	Input / Output	Description
CLKIN	Input	Register Input Clock
DI	Input	Clock enable, Titan2 does not support
CLKOUT	output	Register Output Clock

Table 18 GTP_CLKBUFXCE parameter description

Parameter name	Parameter Type	Valid value	Defaults	Functional description
GATE_EN	<string>	<"FALSE", "TRUE">	<"FALSE">	Titan2 can only be configured as "FALSE"

The timing diagram of the GTP_IOCLKBUF port is shown in the following figure:

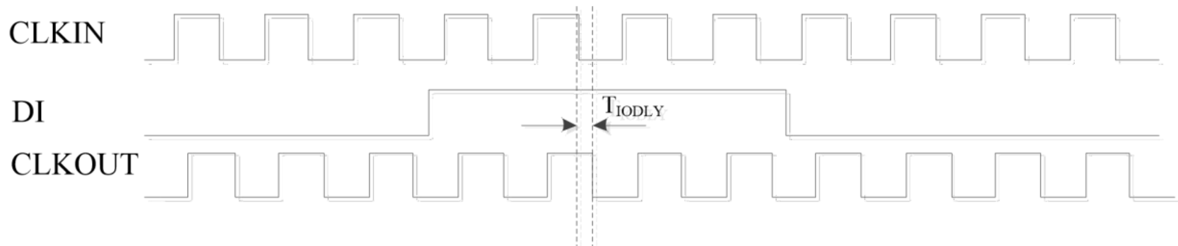


Figure 29 GTP_IOCLKBUF port timing diagram

The GTP_IOCLKBUF of Titan2 series devices only supports the buffer function, and the parameter configuration GATE_EN can only be configured as "FALSE", and does not support DI to control the clock signal, that is, DI inputs 1 or 0, and CLKOUT outputs a valid clock signal.

Note: TIODLY is the delay time from IOCKB input to output.

6. Cross-region clock resources

6.1 Cross-regional clock network

MRCKB mainly provides the clock network across vertically adjacent clock regions, which has strong anti-interference ability and ensures the reliability of high-speed clock quality applied to IO BANK. Each region has 2 MRCKBs.

The input sources of MRCKB are:

- GMCLK in the same region
- SRB

MRCKB can drive: IOCKB, RCKB in the same region and adjacent vertical regions.

The MRCKB input input connection is shown in the figure below:

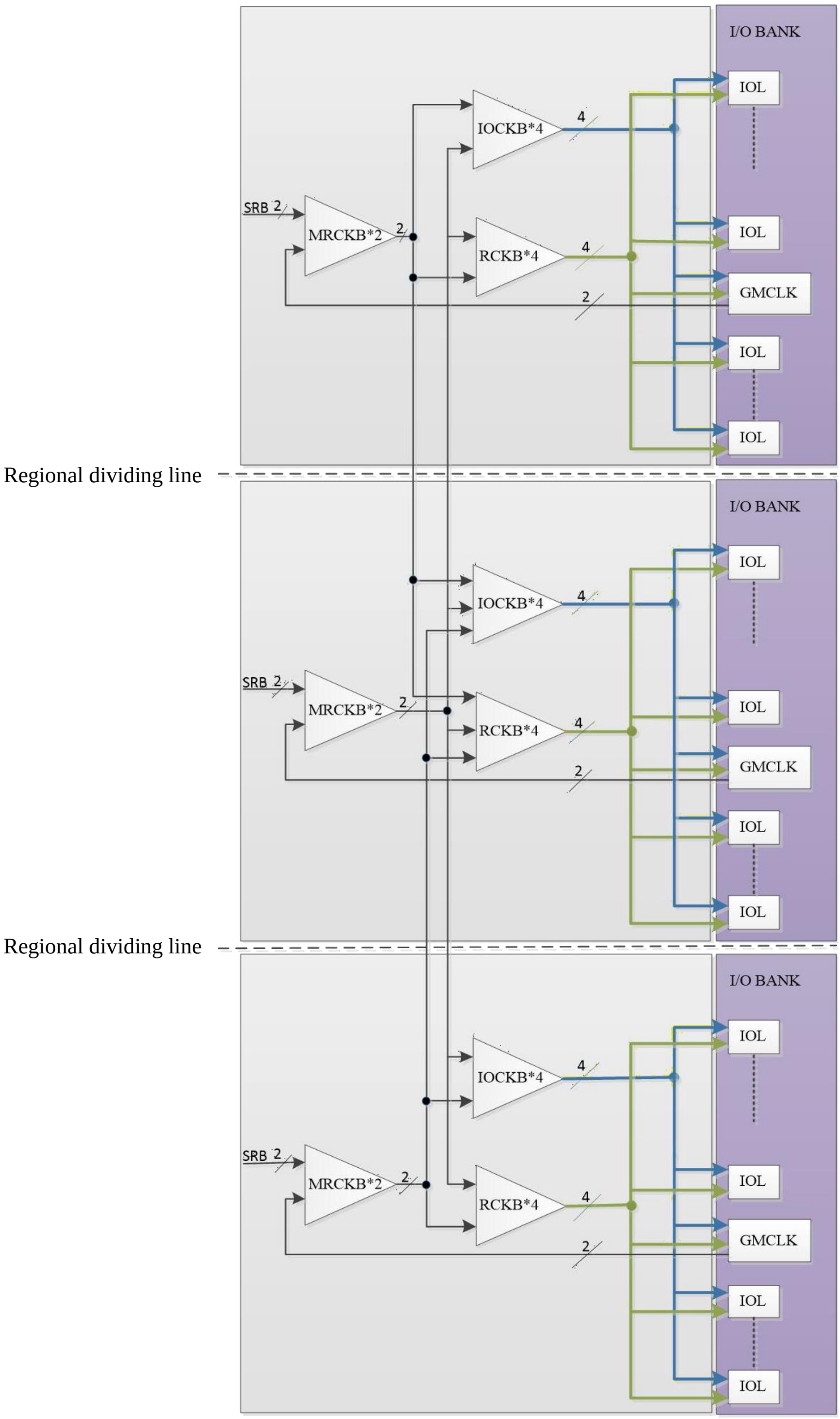


Figure 30 Schematic diagram of MRCKB input clock source and output connection

The above figure is a schematic diagram of the input and output connections of the cross-regional clock buffer. The diagram clearly defines the input clock source of MRCKB, the output drive resources and the reachable area. Since the area where HSSTHP is located does not have MRCKB, IOCKB and RCKB, so except for the area where HSSTHP is located, other areas The MRCKB connection relationship is consistent with that in this Figure. When the external clock is single-ended input, only the GMCLK_P terminal can be used to ensure that the clock signal reaches MRCKB through a dedicated clock path.

6.2 Cross-Region Clock GTP

One cross-regional clock GTP occupies one MRCKB, and a maximum of two are supported in the same region at the same time.

Titan2 series products have two kinds of cross-region clock GTP, one is GTP_CLKBUFM with only input and output; the other is GTP_CLKBUFMCE with frequency division function, which can control whether to output the clock signal by controlling the enable terminal CE.

GTP_CLKBUFM

GTP_CLKBUFM has no parameters, only one input and output, and the output clock frequency is equal to the input clock frequency.

GTP_CLKBUFM primitive instantiation:

```
GTP_CLKBUFM    GTP_CLKBUFM_INST
               (
               .CLKIN     (CLKIN     ),
               .CLKOUT    (CLKOUT    ));
```

GTP_CLKBUFMCE

GTP_CLKBUFMCE has an enable control signal CE, which controls whether the GTP outputs a clock signal. The enable mode (synchronous enable or asynchronous enable) and enable active level (active high or active low) can be set through parameters. And the trigger mode (rising edge trigger or falling edge trigger). In the case of asynchronous enable, when the enable signal CE changes from high to low, the output clock will be pulled down or pulled up immediately, and glitches may occur during switching. In the case of synchronous enable Each switch needs to wait for 2 clock edges (rising edge or falling edge determined by the trigger mode) before switching.

GTP_CLKBUFMCE primitive instantiation:

```
GTP_CLKBUFMCE #(
.CE_TYPE   ("SYNC"     ),
.CE_INV    ("FALSE"    ),
.TRIGGER_MODE ("POSEDGE"   )
) CLKBUFMCE_INST (
.CLKOUT    (CLKOUT     ),
.CE        (CE         ),
.CLKIN     (CLKIN      ) );
```

Table 19 GTP_CLKBUFMCE port description

Port Name	Input Output	Functional description
CLKIN	Input	Input clock signal
CE	Input	Clock enable terminal
CLKOUT	Output	Output clock signal

Table 20 GTP_CLKBUFMCE parameter description

Parameter name	Parameter Type	Valid value	Defaults	Functional description
CE_TYPE	<string>	"SYNC" or "ASYNC"	"SYNC"	CE_TYPE= "SYNC", support synchronous enable. CE_TYPE= "ASYNC", support asynchronous enable.
TRIGGER_MODE	<string>	"POSEDGE" or "NEGEDGE"	"POSEDGE"	TRIGGER_MODE = "POSEDGE", support clock output initial value equal to 1'b1, rising edge trigger. TRIGGER_MODE = "NEGEDGE", support clock output initial value equal to 1'b0, falling edge trigger.
CE_INV	<string>	"TRUE" or "FALSE"	"FALSE"	EN_INV= "FALSE", the default CE is active high. EN_INV="TRUE", the default CE is active low.

Table 21 GTP_CLKBUFMCE mode description

CE_TYPE	TRIGGER_MODE	CE_INV	Function
"SYNC"	"POSEDGE"	"FALSE"	Rising edge synchronous enable mode
"SYNC"	"NEGEDGE"	"FALSE"	Falling Edge Synchronous Enable Mode
"ASYNC"	"NEGEDGE"	"FALSE"	Asynchronous enable mode 0
"ASYNC"	"POSEDGE"	"FALSE"	Asynchronous Enable Mode 1

1. Synchronous enable mode

When configured as rising edge trigger synchronization enable, the output clock is triggered by the rising edge of the input clock, and the output clock remains high when the enable is invalid; when configured as falling edge trigger synchronization enable, the output clock is triggered by the input clock The falling edge of the clock is triggered, and the output clock remains low when the enable is invalid.

The port timing is shown in the following figure:

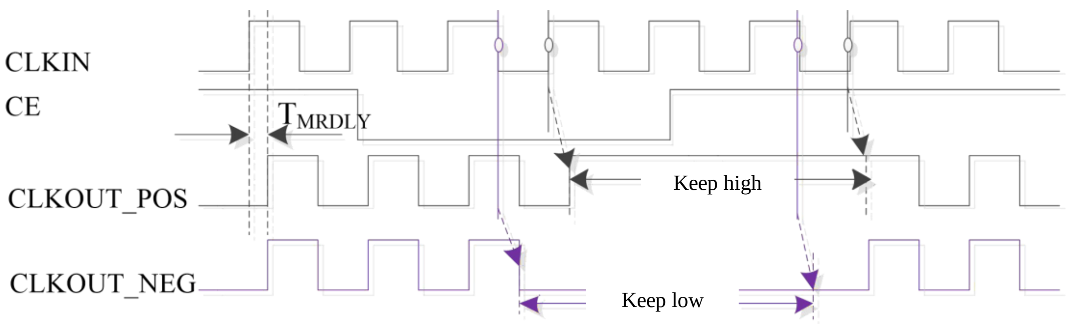


Figure 31 GTP_CLKBUFMCE port timing diagram1

CLKOUT_POS represents the output clock when TRIGGER_MODE = "POSEDGE", CLKOUT_NEG represents the output clock when TRIGGER_MODE = "NEGEDGE", the dotted arrow indicates the clock switching time, and the default CE is active high.

2. Asynchronous enable mode

When configured as asynchronous enable, the output clock switches immediately when the enable signal CE switches. In this case, glitches may occur. The port timing is shown in the following figure:

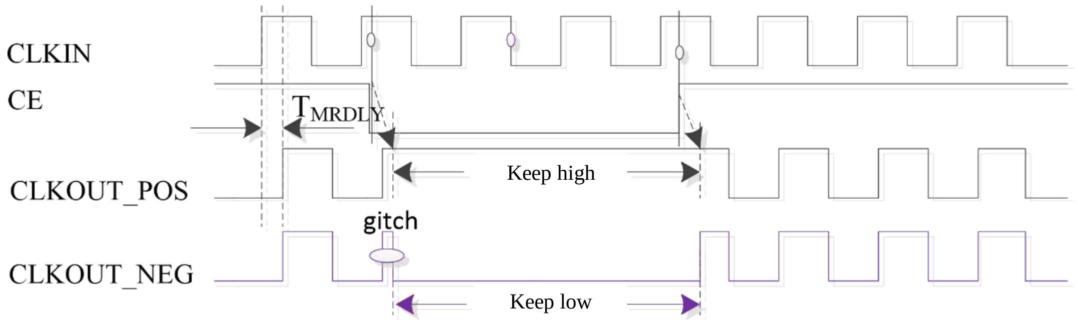


Figure 32 GTP_CLKBUFMCE port timing diagram2

CLKOUT_POS represents the output clock when TRIGGER_MODE = "POSEDGE", CLKOUT_NEG represents the output clock when TRIGGER_MODE = "NEGEDGE", the dotted arrow indicates the clock switching time, and the default CE is active at high level.

6.3 Cross-Regional Clock Application

MRCKB drives multiple IOCKBs

When spanning 3 vertically adjacent areas and only driving IOL (IO logic resources), MRCKB can be used to drive 3 IOCKBs. Although RCKB can also drive IOLs, because the IO clock network provides high-quality high-speed clocks, it is usually selected to implement IOCKB, the corresponding GTP needs to be instantiated, as shown in the following figure:

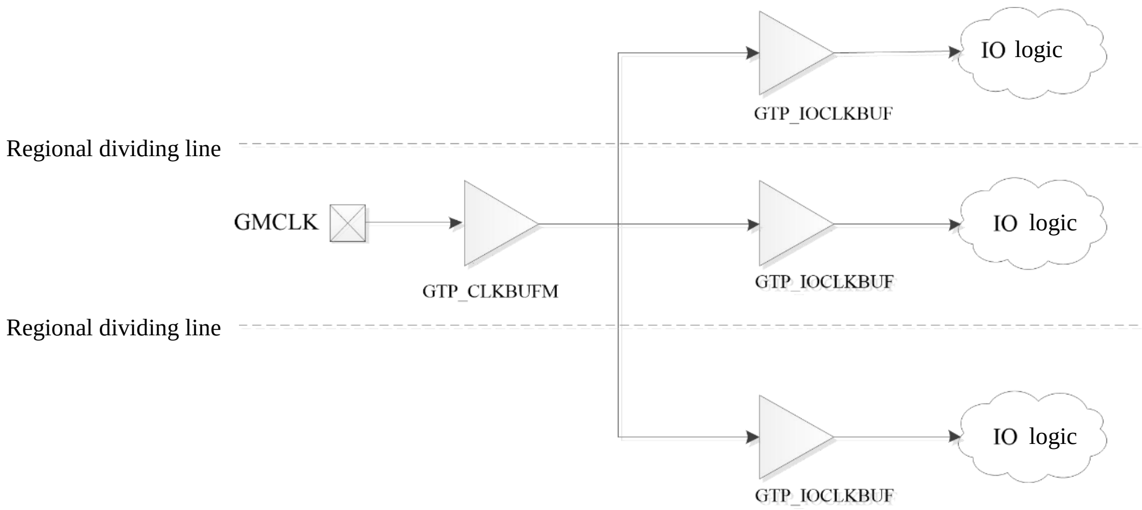


Figure 33 MRCKB drives multiple IOCKBs

The position of GTP_IOCLKBUF can be manually constrained to an RCKB.

MRCKB drives multiple RCKB

When the same clock spans three vertically adjacent areas and drives the IOL and the logic resources of these three areas, MRCKB can be used to drive three RCKBs. At this time, the clock frequency output to the outside of the device is the same as the clock frequency driving the internal logic. The corresponding GTP needs to be instantiated, as shown in the following figure:

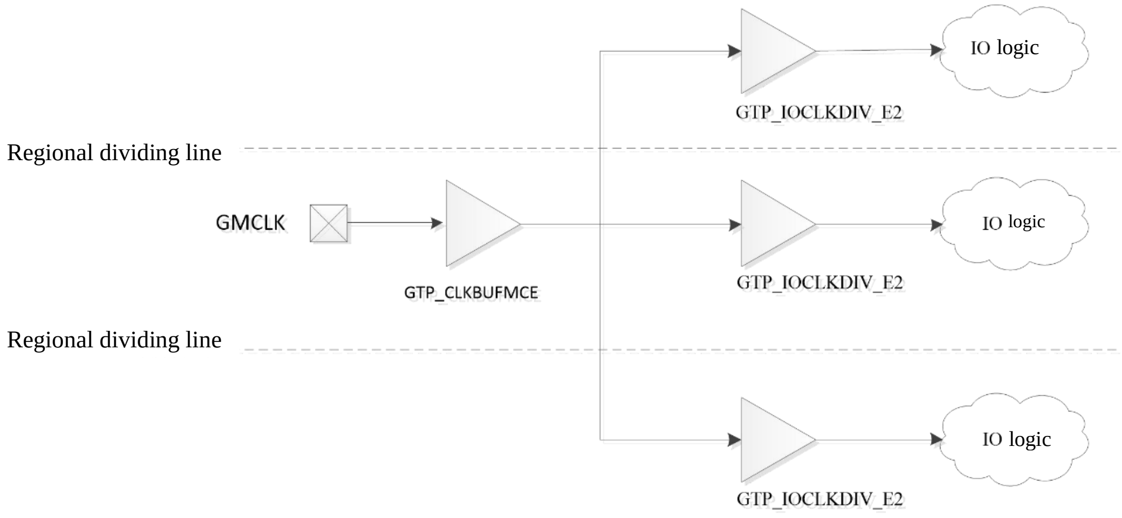


Figure 34 MRCKB drives multiple RCKB

If GTP_IOCLKDIV_E2 uses the frequency division function, when GTP_CLKBUFMCE is disabled and the output clock is turned off, GTP_IOCLKDIV_E2 needs to be reset and cleared.

MRCKB drives multiple RCKBs and IOCKBs

MRCKB can be used in conjunction with RCKB and IOCKB to drive ISERDES and OSERDES. RCKB is connected to the low-speed clock terminal through frequency division, and IOCKB is connected to the high-speed clock terminal. The corresponding GTP needs to be instantiated, as shown in the following figure:

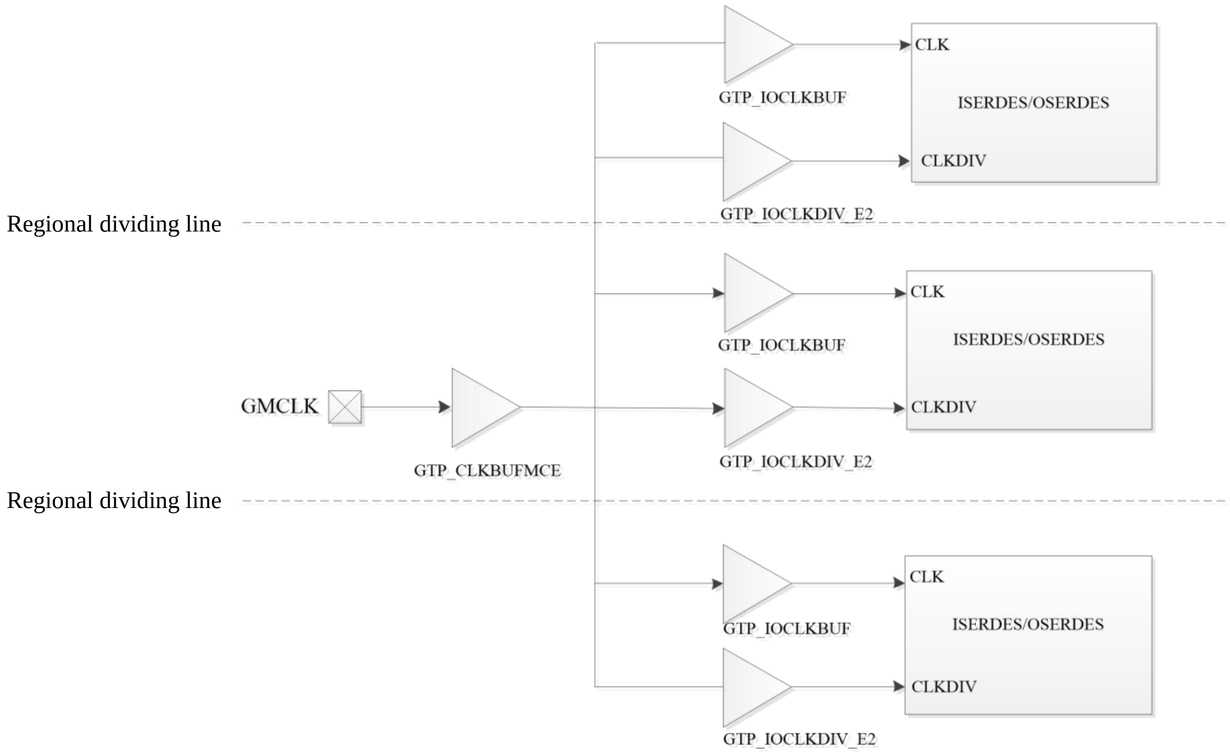


Figure 35 MRCKB drives multiple IOCKB and RCKB

Assuming that the input clock frequency is 300MHz, after passing through GTP_CLKBUFMCE from the clock pin GMCLK (if it is a single-ended input, it can only be GMCLK_P), one way passes through GTP_IOCLKDIV_E2 to divide the frequency by 2 to obtain a 150MHz clock. The regional clock network connects to the clock port CLKDIV, and the other way passes through the GTP_IOCLKBUF The 300MHz clock is connected to the clock port CLK through the IO clock network.

If the IO clock network is not enough, you can also replace GTP_IOCLKBUF with GTP_IOCLKDIV_E2 / GTP_CLKBUFR.

7. PLL clock resources

The input sources of Titan2 GPLL and PPLL (CLKIN1, CLKIN2, CLKFB) are:

- GMCLK and GSCLK for left or right half
- USCM
- RCKB in the same area
- HCKB in the same region
- GPLL/PPLL CLKOUT0~3/N
- HSSTHP clock (see Chapter 1, Section 4, Clock Connection Overview)

Note: The clock coming in from the clock pins GMCLK and GSCLK can also reach the GPLL/PPLL in the left and right halves, but it can only pass through USCM.

Drivers are:

GPLL:

- CLKOUT0~3/N, CLKOUT4~6, CLKOUTF/CLKOUTFN: the same upper/lower half area USCM and the same area HCKB;
- CLKOUT0~3: RCKB and IOCKB in the same area;

PPLL:

- CLKOUT0/N, CLKOUT1~4, CLKOUTF/CLKOUTFN: the same upper/lower half area USCM and the same area HCKB;
- CLKOUT0~3: RCKB and IOCKB in the same area;
- CLKOUTPHY/N:DDR PHY;

Since HSSTHP does not have GPLL and PPLL, the HSSTHP output clock as its input clock source must reach GPLL/PPLL through USCM or HCKB, and BUFG (such as GTP_CLKBUFG) or BUFX (such as GTP_CLKBUFX) needs to be inserted. HSSTCLK includes 4-way P_RCLK2FABRIC, 4-way P_TCLK2FABRIC and The clock after 2-way reference clock PAD_REFCLKP/N is converted to single-ended.

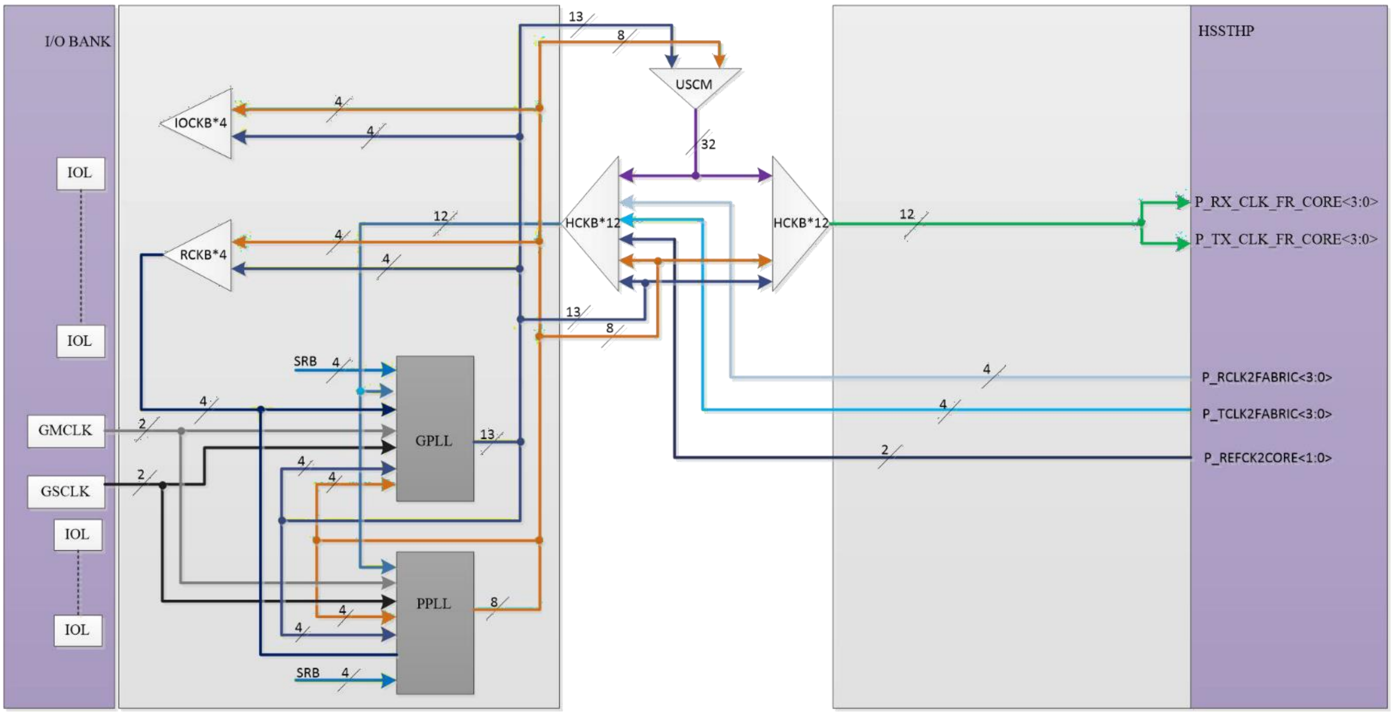


Figure 36 PLL Input Clock Source and Output Clock Connection Diagram

Through the PLL clock trunk or clock tree (RCKB, HCKB), CLKOUT0~3 of PPLL, GPLL can be used as the input clock of PPLL, GPLL in other PLL, and then complete the cascading of PLL.

(2) GPLL instructions

1. GPLL overview

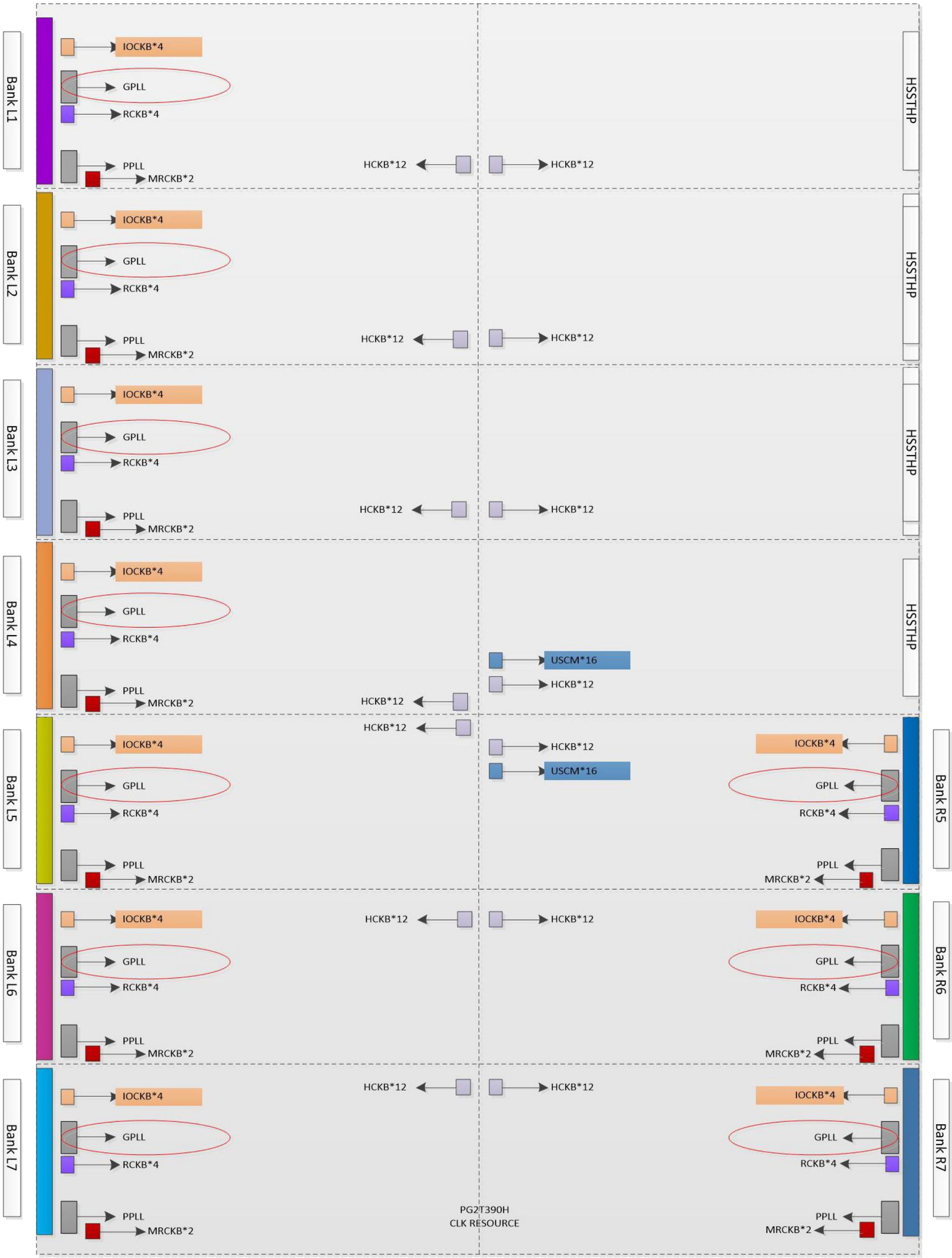


Figure 37 GPLL resource diagram (Top View)

There are 10 GPLLs in PG2T390H, except for the 4 areas of HSSTHP, each other clock area has 1 GPLL, as shown in the red circle in Figure 37. GPLL mainly has the following characteristics: clock frequency synthesis, clock SKEW reduction, phase adjustment , spread spectrum output, clock cascading, output clock gating, APB dynamic reconfiguration, etc.

The block diagram of the GTP_GPLL system is shown in the figure below.

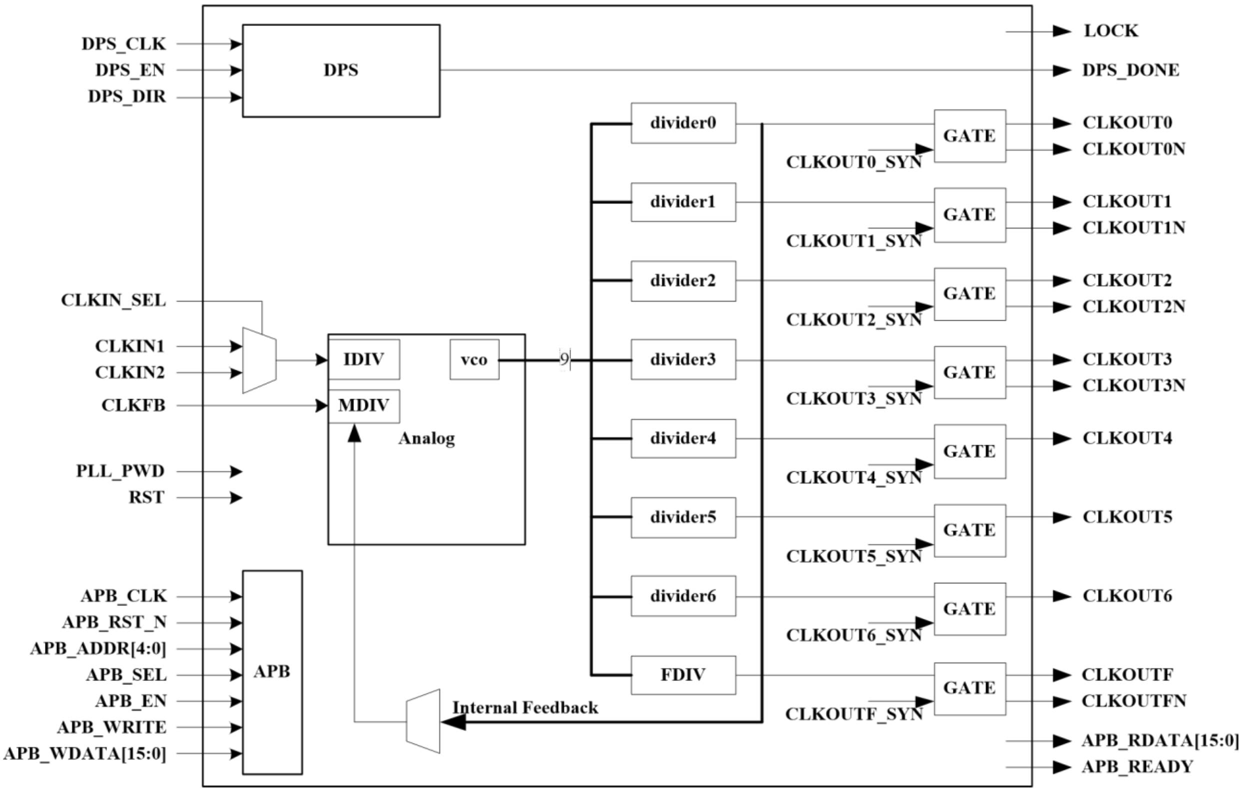


Figure 38 GPLL System Block Diagram

In use, by calling the instance configuration of GTP_GPLL, the output shutdown can be configured for unused output ports to reduce power consumption. The application of GTP_GPLL is introduced below.

2. GTP_GPLL top-level block diagram

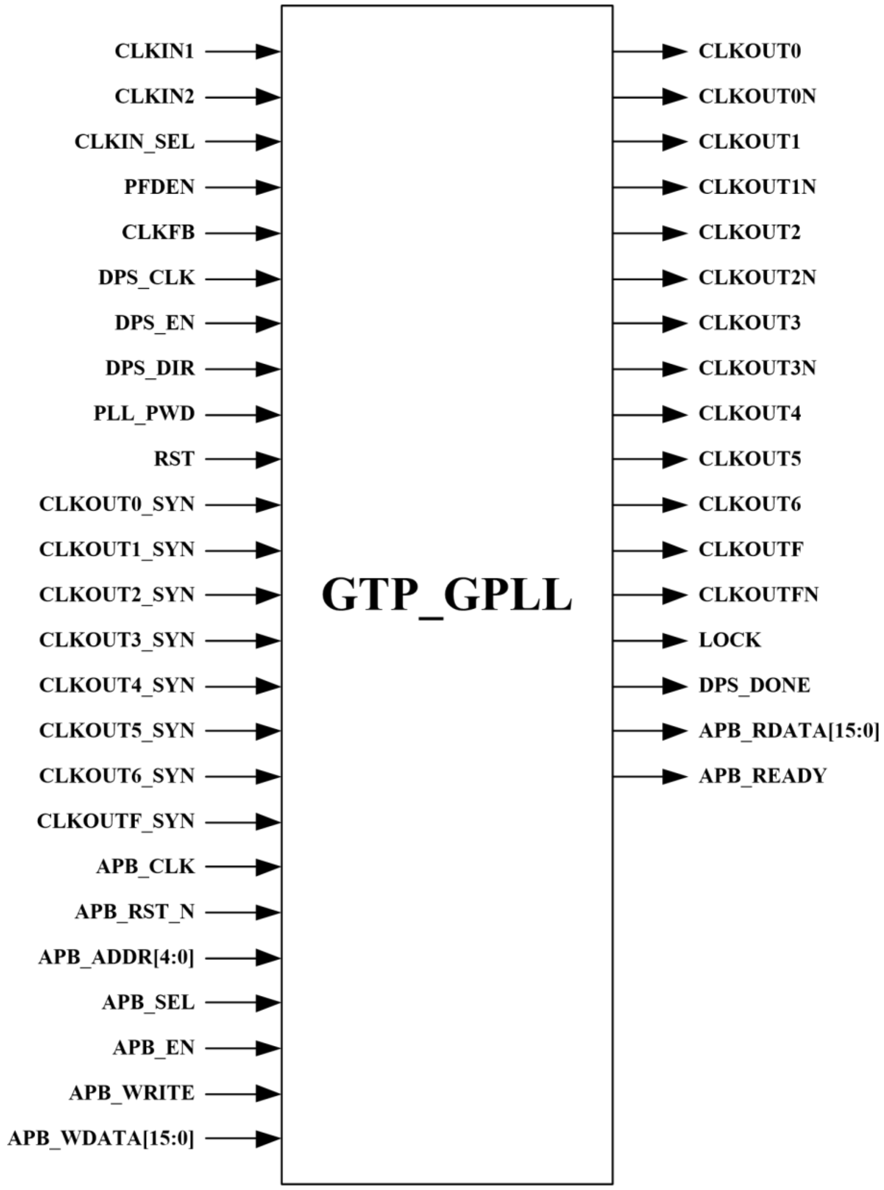


Figure 39 GTP_GPLL block diagram

3. GTP_GPLL port list

Table 22 GTP_GPLL port description

Port	I/O	Functional description
CLKOUT0	O	The positive phase output clock of the 0th channel of PLL;
CLKOUT0N	O	PLL channel 0 inverted output clock;
CLKOUT1	O	PLL No. 1 non-inverting output clock;
CLKOUT1N	O	PLL 1st channel inverted output clock;
CLKOUT2	O	PLL No. 2 non-inverting output clock;
CLKOUT2N	O	PLL No. 2 inverted output clock;
CLKOUT3	O	PLL No. 3 positive phase output clock;
CLKOUT3N	O	PLL No. 3 inverted output clock;
CLKOUT4	O	PLL 4th output clock;
CLKOUT5	O	PLL 5th output clock;

Port	I/O	Functional description
CLKOUT6	O	PLL 6th output clock;
CLKOUTF	O	PLL feedback positive phase output clock;
CLKOUTFN	O	PLL feedback inverting output clock;
LOCK	O	PLL frequency lock indication signal, which is an asynchronous signal; When the signal is pulled high, it indicates that the PLL feedback clock signal has been locked to the input clock signal;
DPS_DONE	O	Dynamic interpolation phase shift adjustment indication signal;
APB_RDATA[15:0]	O	PLL APB interface data bus data output;
APB_READY	O	PLL APB interface data bus handshake signal; indicates the end of a normal bus cycle;
CLKIN1	I	PLL main reference clock input;
CLKIN2	I	PLL secondary reference clock input;
CLKFB	I	PLL feedback clock input;
CLKIN_SEL	I	input clock selection signal;
DPS_CLK	I	Dynamic interpolation phase shift adjustment clock;
DPS_EN	I	Dynamic interpolation phase shift adjustment enable; active high;
DPS_DIR	I	Select the direction of dynamic interpolation phase shift adjustment; 1'b0: lagging, 1'b1: leading;
PLL_PWD	I	PLL Power Down; active high;
RST	I	PLL asynchronous reset signal, active high;
CLKOUT0_SYN	I	CLKOUT0/N output clock enable control; high level active; high level off, low level enable;
CLKOUT1_SYN	I	CLKOUT1/N output clock enable control; high level active; high level off, low level enable;
CLKOUT2_SYN	I	CLKOUT2/N output clock enable control; high level active; high level off, low level enable;
CLKOUT3_SYN	I	CLKOUT3/N output clock enable control; high level active; high level off, low level enable;
CLKOUT4_SYN	I	CLKOUT4 output clock enable control; high level active; high level off, low level enable;
CLKOUT5_SYN	I	CLKOUT5 output clock enable control; high level active; high level off, low level enable;
CLKOUT6_SYN	I	CLKOUT6 output clock enable control; high level active; high level off, low level enable;
CLKOUTF_SYN	I	CLKOUTF/N output clock enable control; high level active; high level off, low level enable;
APB_CLK	I	PLL APB interface data bus clock;
APB_RST_N	I	PLL APB interface data bus asynchronous reset signal, active low;
APB_ADDR	I	PLL APB interface data bus address;
APB_SEL	I	PLL APB interface data bus selection signal, select slave device;
APB_EN	I	PLL APB interface data bus enable signal;
APB_WRITE	I	PLL APB interface data bus write enable signal; 1’b0: read operation, 1’b1: write operation;
APB_WDATA[15:0]	I	PLL APB interface data bus data input;

Note:

In the software process, insert BUFG to the GPLL output, and give priority to the global clock network. If you want to change the clock network, you can set it through the PAP_CLOCK_ASSIGN attribute. For detailed usage, refer to "User_Constraint_Editor_User_Guide".

3.1 GTP_GPLL detailed description

- CLKIN1

CLKIN1 is the main reference clock input, which can be directly driven by GMCLK and GSCLK in the same area. GMCLK and GSCLK drive all GPLLs on the same left side or right side through the PLL clock tree, can be driven by RCKB and HCKB in the same area, and can also be driven by SRB Driver (not recommended), GPLL can be cascaded, CLKOUT0~3/N can be used as CLKIN1 input to realize cascading.

- CLKIN2

CLKIN2 is a secondary input clock that is often used in applications that dynamically switch reference clocks. CLKIN2 can be directly driven by GMCLK and GSCLK in the same area, or GMCLK and GSCLK can drive all GPLLs on the same left or left side through the PLL clock tree, It can be driven by RCKB and HCKB in the same area, and can also be driven by SRB (not recommended). CLKOUT0~3/N can be used as CLKIN2 input to realize cascading.

- CLKFB

CLKFB Feedback clock input, connected with external feedback output clock CLKOUTF as FPGA internal feedback, or through clock input pin GMCLK/GSCLK, connected to feedback clock input CLKFB via GCLK_IBUF/USCM/HCKB as GPLL feedback clock, can be used for external clock alignment (Reference clock and feedback clock need to go through the same type of clock buffer).

- CLKOUTF

Feedback clock output, supports variable duty cycle, variable frequency (supports fractional frequency division), phase adjustment (only supported as an ordinary clock output port, phase cannot be adjusted when used as a feedback clock) and can be turned off or on, and can drive USCM /HCKB, see the GTP_GPLL application mode in Section 8 of this chapter for conventional applications.

- CLKOUTFN

The inverted output clock of CLKOUTF cannot be used as a feedback output clock.

- CLKIN_SEL

Select the input reference clock control signal, CLKIN_SEL=0, CLKIN1 is selected, CLKIN_SEL=1, CLKIN2 is selected, and the GPLL needs to be reset when the input clock is switched.

- PLL_PWD

Power-off control signal, when some modules do not need to work, the GPLL can be turned off to reduce power consumption.

- APB configuration interface

The APB interface is a dynamic configuration interface, which can configure the output clock frequency, phase, duty cycle, etc. For details, please refer to the GPLL APB interface configuration in Section 5 of this chapter. When using the dynamic configuration function, you need to reset the GPLL and must operate according to the specified interface timing, otherwise the configuration may be abnormal.

- DPS interface

The DPS interface is used to realize the dynamic phase modulation function, please refer to the phase adjustment dynamic adjustment part in section 6.8 of this chapter for details.

- CLKOUT0~6_SYN, CLKOUTF_SYN

Output clock enable signal, turn off the output clock at a high level, when the module driven by a certain clock output by the GPLL does not need to work, the clock can be turned off, and the clock is not provided to the module, which can reduce power consumption.

- CLKOUT0~6

Output clock interface, each output clock is obtained by VCO frequency division (see Figure 38 for details), the default phase alignment, each channel supports phase shift, variable duty cycle, variable frequency and can be turned off or on , only CLKOUT0 supports fractional frequency division.

When the GPLL output clock is to drive RCKB or IOCKB, only CLKOUT0~3 can be selected, and these 6

outputs can drive USCM and HCKB; CLKOUT0~3 output can also be used as other GPLL/PPLL input with the PLL clock tree, to achieve link function.

- CLKOUT0~3N

CLKOUT0~3N is the 180° reverse clock output of CLKOUT0~3.

- LOCK

The LOCK signal is used to indicate when the phase alignment of the input reference clock (CLKIN1/CLKIN2) and the feedback input clock has been locked to the input clock signal.

4. GTP_GPLL parameter list

Table 23 GTP_GPLL parameter description

Parameter name	Parameter Type	Valid value	Defaults	Functional description
CLKIN_FREQ	real	10~800	50.0	Input clock frequency configuration, MHz;
LOCK_MODE	binary	1'b0, 1'b1	1'b0	PLL frequency detection mode configuration; 1'b0: Real-time monitoring of PLL working status; 1'b1: LOCK 1 is kept after PLL is locked, unless reset or Power Down;
STATIC_RATIOI	interger	1-80	1	Enter the divider ratio static configuration;
STATIC_RATIOM	interger	1-128	1	Feedback M divider ratio static configuration;
STATIC_RATIO0	real	1-128 or 2.000~128.000, step 0.125	1.0	Output divider0 ratio static configuration; integer frequency division mode, support 1~128; Fractional frequency division mode, support 2.000~128.000;
STATIC_RATIO1	interger	1-128	1	Output divider1 ratio static configuration;
STATIC_RATIO2	interger	1-128	1	Output divider2 ratio static configuration;
STATIC_RATIO3	interger	1-128	1	Output divider3 ratio static configuration;
STATIC_RATIO4	interger	1-128	1	Output divider4 ratio static configuration;
STATIC_RATIO5	interger	1-128	1	Output divider5 ratio static configuration;
STATIC_RATIO6	interger	1-128	1	Output divider6 ratio static configuration;
STATIC_RATIOF	real	1-128 or 2.000~128.000 step 0.125	1.0	Feedback F divider ratio static configuration; integer frequency division mode, support 1~128; Fractional frequency division mode, support 2.000~128.000;
STATIC_DUTY0	interger	2~255	2	Output divider0 duty static configuration;
STATIC_DUTY1	interger	2~255	2	Output divider1 duty static configuration;
STATIC_DUTY2	interger	2~255	2	Output divider2 duty static configuration;
STATIC_DUTY3	interger	2~255	2	Output divider3 duty static configuration;
STATIC_DUTY4	interger	2~255	2	Output divider4 duty static configuration;
STATIC_DUTY5	interger	2~255	2	Output divider5 duty static configuration;
STATIC_DUTY6	interger	2~255	2	Output divider6 duty static configuration;
STATIC_DUTYF	interger	2~255	2	Feedback F divider duty static configuration;
STATIC_PHASE	interger	0-63	0	Interpolation phase shift phase static configuration;
STATIC_PHASE0	interger	0-7	0	Output divider0 fine phase static configuration;
STATIC_PHASE1	interger	0-7	0	Output divider1 fine phase static configuration;

Parameter name	Parameter Type	Valid value	Defaults	Functional description
STATIC_PHASE2	interger	0-7	0	Output divider2 fine phase static configuration;
STATIC_PHASE3	interger	0-7	0	Output divider3 fine phase static configuration;
STATIC_PHASE4	interger	0-7	0	Output divider4 fine phase static configuration;
STATIC_PHASE5	interger	0-7	0	Output divider5 fine phase static configuration;
STATIC_PHASE6	interger	0-7	0	Output divider6 fine phase static configuration;
STATIC_PHASEF	interger	0-7	0	Feedback F divider fine phase static configuration;
STATIC_CPHASE0	interger	0-127	0	Output divider0 coarse phase static configuration;
STATIC_CPHASE1	interger	0-127	0	Output divider1 coarse phase static configuration;
STATIC_CPHASE2	interger	0-127	0	Output divider2 coarse phase static configuration;
STATIC_CPHASE3	interger	0-127	0	Output divider3 coarse phase static configuration;
STATIC_CPHASE4	interger	0-127	0	Output divider4 coarse phase static configuration;
STATIC_CPHASE5	interger	0-127	0	Output divider5 coarse phase static configuration;
STATIC_CPHASE6	interger	0-127	0	Output divider6 coarse phase static configuration;
STATIC_CPHASEF	interger	0-127	0	Feedback F divider coarse phase static configuration;
CLK_DPS0_EN	string	"FALSE", "TRUE"	"FALSE"	Output divider0 interpolation phase shift enable;
CLK_DPS1_EN	string	"FALSE", "TRUE"	"FALSE"	Output divider1 interpolation phase shift enable;
CLK_DPS2_EN	string	"FALSE", "TRUE"	"FALSE"	Output divider2 interpolation phase shift enable;
CLK_DPS3_EN	string	"FALSE", "TRUE"	"FALSE"	Output divider3 interpolation phase shift enable;
CLK_DPS4_EN	string	"FALSE", "TRUE"	"FALSE"	Output divider4 interpolation phase shift enable;
CLK_DPS5_EN	string	"FALSE", "TRUE"	"FALSE"	Output divider5 interpolation phase shift enable;
CLK_DPS6_EN	string	"FALSE", "TRUE"	"FALSE"	Output divider6 interpolation phase shift enable;
CLK_DPSF_EN	string	"FALSE", "TRUE"	"FALSE"	Feedback F divider interpolation phase shift enable;
CLK_CAS5_EN	string	"FALSE", "TRUE"	"FALSE"	Output divider5 clock cascade enable;
CLKOUT0_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUT0_SYN signal enable configuration;
CLKOUT1_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUT1_SYN signal enable configuration;
CLKOUT2_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUT2_SYN signal enable configuration;
CLKOUT3_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUT3_SYN signal enable configuration;
CLKOUT4_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUT4_SYN signal enable configuration;
CLKOUT5_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUT5_SYN signal enable configuration;
CLKOUT6_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUT6_SYN signal enable configuration;
CLKOUTF_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUTF_SYN signal enable configuration;
SSC_MODE	string	"DOWN_LOW", "DOWN_HIGH", "CENTER_LOW", "CENTER_HIGH", "DISABLE"	"DISABLE"	SSC mode configuration;
SSC_FREQ	real	25~250	50.0	SSC modulation frequency configuration, KHz;
INTERNAL_FB	string	"CLKOUT0", "CLKOUT1", "CLKOUT2", "CLKOUT3", "CLKOUT4", "CLKOUT5", "CLKOUT6", "CLKOUTF", "DISABLE"	"CLKOUTF"	Internal feedback path selection, select one of these output clocks as the internal feedback clock, such as INTERNAL_FB = " CLKOUT0", then the output Clock CLKOUT0 as internal feedback clock;

Parameter name	Parameter Type	Valid value	Defaults	Functional description
EXTERNAL_FB	string	"CLKOUT0", "CLKOUT1" "CLKOUT2", "CLKOUT3", "CLKOUT4", "CLKOUT5" "CLKOUT6", "CLKOUTF", "DISABLE"	"DISABLE"	External feedback path selection, select one of these output clocks as the external feedback clock, such as EXTERNAL_FB = " CLKOUT0", then the output clock CLKOUT0 is used as the internal feedback clock;
BANDWIDTH	string	"LOW", "HIGH" "OPTIMIZED"	"OPTIMIZED"	Bandwidth selection configuration: BANDWIDTH="LOW" is configured as "LOW", BANDWIDTH="HIGH" is configured as "HIGH" BANDWIDTH="OPTIMIZED" is configured as "OPTIMIZED";

Note:

(1) Parameters CLK_DPS5_EN and CLK_CAS5_EN cannot be configured as "TRUE" at the same time;

(2) The parameters INTERNAL_FB and EXTERNAL_FB cannot be configured as "DISABLE" at the same time;

(3) PFD configured with "LOW", "OPTIMIZED" and "HIGH" of BANDWIDTH is limited by PFD frequency, see Table 38 for details;

5. GTP_GPLL APB interface configuration

5.1 Configuration interface

The user logic dynamically changes the GTP_GPLL working parameters through the APB interface. The sequence of reading and writing registers of the APB interface is shown in Figure 40~Figure 43.

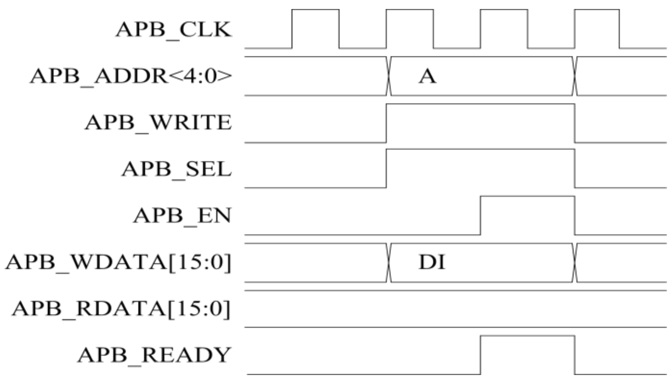


Figure 40 GTP_PPLL_APB Write Timing

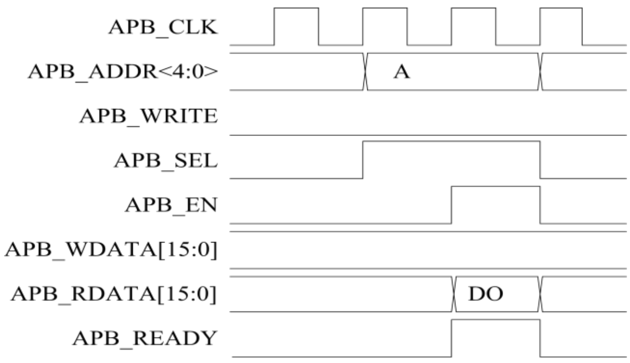


Figure 41 GTP_PPLL_APB Read Timing

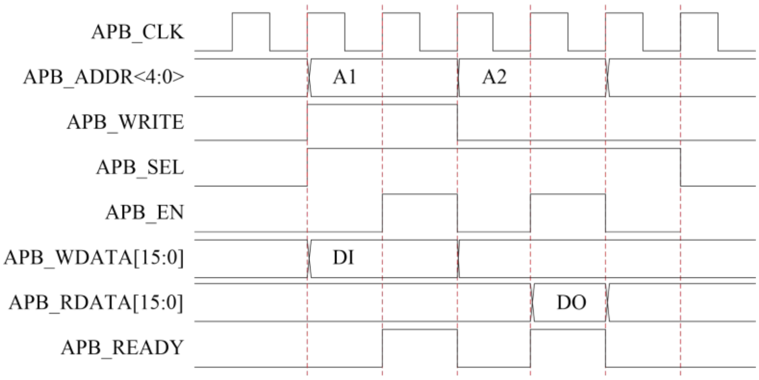


Figure 42 GTP_PPLL_APB read-after-write timing

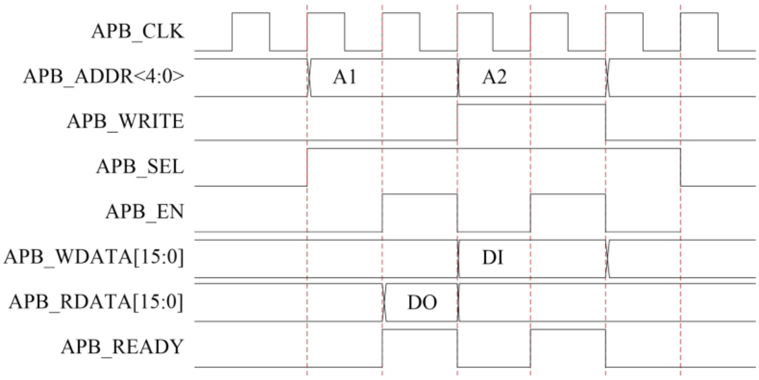


Figure 43 GTP_PPLL_APB interface read-after-write timing

Table 24 GTP_GPLL_APB port description

Serial number	Port name	I/O	Description
1	APB_CLK	I	Clock, rising edge sampling;
2	APB_RST_N	I	Asynchronous reset, active low; only reset Data Bus (do not reset registers);
3	APB_ADDR[4:0]	I	Address bus;
4	APB_SEL	I	Selected, indicating that the slave device is selected;
5	APB_EN	I	Enable, bus enable signal;
6	APB_WRITE	I	Direction, 0: read, 1: write;
7	APB_WDATA[15:0]	I	Data bus input;
8	APB_RDATA[15:0]	O	Data bus output;
9	APB_READY	O	Flag signal, high effective;

System application requirements for writing internal registers via APB interface:

(1) After the APB rewrites the internal registers, it is necessary to reset the PLL to ensure its normal operation;

(2) The minimum pulse width of TRST is 10ns;

5.2 Configuration registers

Table 25 GTP_GPLL APB interface register description

APB_ADDR[4:0]	Bit	Register	Description
0	[15:8]	REG_ODIV0_RATIO[7:0]	ODIV0 Register1: frequency division ratio setting;
	[7:0]	REG_ODIV0_DUTY[7:0]	ODIV0 Register1: duty cycle setting;
1	[15:13]	REG_ODIV0_FRACDIV_RATIO[2:0]	ODIV0 Register2: Fraction setting for fraction frequency division;
	[12:10]	REG_ODIV0_FRACDIV_PSOFFSET[2:0]	ODIV0 Register2: fractional frequency division falling edge phase setting;
	[9:7]	REG_ODIV0_FPHASE[2:0]	ODIV0 Register2: phase fine adjustment setting;

APB_ADDR[4:0]	Bit	Register	Description
	[6:0]	REG_ODIV0_CPHASE[6:0]	ODIV0 Register2: coarse phase adjustment setting;
2	[15:6]	RESERVED	ODIV0 Register3
	[5:4]	REG_ODIV0_ADJUST[1:0]	ODIV0 Register3: Fractional frequency division timing adjustment setting;
	[3]	REG_ODIV0_FRACDIV_EN	ODIV0 Register3: fractional frequency division enable;
	[2:1]	REG_ODIV0_DPSORCAS_SEL[1:0]	ODIV0 Register3: input clock selection;
	[0]	REG_ODIV0_MUXSEL_EN	ODIV0 Register3: input clock MUX enable;
3	[15:8]	REG_ODIV1_RATIO[7:0]	ODIV1 Register1: frequency division ratio setting;
	[7:0]	REG_ODIV1_DUTY[7:0]	ODIV1 Register1: duty cycle setting;
4	[15:13]	RESERVED	
	[12:11]	REG_ODIV1_DPSORCAS_SEL[1:0]	ODIV1 Register2: input clock selection;
	[10]	REG_ODIV1_MUXSEL_EN	ODIV1 Register2: input clock MUX enable;
	[9:7]	REG_ODIV1_FPHASE[2:0]	ODIV1 Register2: phase fine adjustment setting;
	[6:0]	REG_ODIV1_CPHASE[6:0]	ODIV1 Register2: coarse phase adjustment setting;
5	[15:8]	REG_ODIV2_RATIO[7:0]	ODIV2 Register1: frequency division ratio setting;
	[7:0]	REG_ODIV2_DUTY[7:0]	ODIV2 Register1: duty cycle setting;
6	[15:13]	RESERVED	
	[12:11]	REG_ODIV2_DPSORCAS_SEL[1:0]	ODIV2 Register2: input clock selection;
	[10]	REG_ODIV2_MUXSEL_EN	ODIV2 Register2: input clock MUX enable;
	[9:7]	REG_ODIV2_FPHASE[2:0]	ODIV2 Register2: phase fine adjustment setting;
	[6:0]	REG_ODIV2_CPHASE[6:0]	ODIV2 Register2: coarse phase adjustment setting;
7	[15:8]	REG_ODIV3_RATIO[7:0]	ODIV3 Register1: frequency division ratio setting;
	[7:0]	REG_ODIV3_DUTY[7:0]	ODIV3 Register1: duty cycle setting;
8	[15:13]	RESERVED	
	[12:11]	REG_ODIV3_DPSORCAS_SEL[1:0]	ODIV3 Register2: input clock selection;
	[10]	REG_ODIV3_MUXSEL_EN	ODIV3 Register2: input clock MUX enable;
	[9:7]	REG_ODIV3_FPHASE[2:0]	ODIV3 Register2: phase fine adjustment setting;
	[6:0]	REG_ODIV3_CPHASE[6:0]	ODIV3 Register2: coarse phase adjustment setting;
9	[15:8]	REG_ODIV4_RATIO[7:0]	ODIV4 Register1: frequency division ratio setting;
	[7:0]	REG_ODIV4_DUTY[7:0]	ODIV4 Register1: duty ratio setting;
A	[15:13]	RESERVED	
	[12:11]	REG_ODIV4_DPSORCAS_SEL[1:0]	ODIV4 Register2: input clock selection;
	[10]	REG_ODIV4_MUXSEL_EN	ODIV4 Register2: input clock MUX enable;
	[9:7]	REG_ODIV4_FPHASE[2:0]	ODIV4 Register2: Phase fine-tuning setting;
	[6:0]	REG_ODIV4_CPHASE[6:0]	ODIV4 Register2: coarse phase adjustment setting;
B	[15:8]	REG_ODIV5_RATIO[7:0]	ODIV5 Register1: frequency division ratio setting;
	[7:0]	REG_ODIV5_DUTY[7:0]	ODIV5 Register1: duty cycle setting;
C	[15:13]	RESERVED	
	[12:11]	REG_ODIV5_DPSORCAS_SEL[1:0]	ODIV5 Register2: input clock selection;
	[10]	REG_ODIV5_MUXSEL_EN	ODIV5 Register2: input clock MUX enable;
	[9:7]	REG_ODIV5_FPHASE[2:0]	ODIV5 Register2: Phase fine-tuning setting;
	[6:0]	REG_ODIV5_CPHASE[6:0]	ODIV5 Register2: coarse phase adjustment setting;
D	[15:8]	REG_ODIV6_RATIO[7:0]	ODIV6 Register1: frequency division ratio setting;
	[7:0]	REG_ODIV6_DUTY[7:0]	ODIV6 Register1: duty cycle setting;
E	[15:13]	RESERVED	
	[12:11]	REG_ODIV6_DPSORCAS_SEL[1:0]	ODIV6 Register2: input clock selection;
	[10]	REG_ODIV6_MUXSEL_EN	ODIV6 Register2: input clock MUX enable;

APB_ADDR[4:0]	Bit	Register	Description
	[9:7]	REG_ODIV6_FPHASE[2:0]	ODIV6 Register2: phase fine adjustment setting;
	[6:0]	REG_ODIV6_CPHASE[6:0]	ODIV6 Register2: coarse phase adjustment setting;
F	[15:8]	REG_FDIV_RATIO[7:0]	FDIV Register1: frequency division ratio setting;
	[7:0]	REG_FDIV_DUTY[7:0]	FDIV Register1: duty cycle setting;
10	[15:13]	REG_FDIV_FRACDIV_RATIO[2:0]	FDIV Register2: Fractional setting of fractional frequency division;
	[12:10]	REG_FDIV_FRACDIV_PSOFFSET[2:0]	FDIV Register2: fractional frequency division falling edge phase setting;
	[9:7]	REG_FDIV_FPHASE[2:0]	FDIV Register2: phase fine adjustment setting;
	[6:0]	REG_FDIV_CPHASE[6:0]	FDIV Register2: coarse phase adjustment setting;
11	[15:6]	RESERVED	FDIV Register3
	[5:4]	REG_FDIV_ADJUST[1:0]	FDIV Register3: fractional frequency division timing adjustment settings;
	[3]	REG_FDIV_FRACDIV_EN	FDIV Register3: Fractional frequency division enable;
	[2:1]	REG_FDIV_DPSORCAS_SEL[1:0]	FDIV Register3: input clock selection;
	[0]	REG_FDIV_MUXSEL_EN	FDIV Register3: input clock MUX enable;
12	[15:8]	RESERVED	
	[7:0]	REG_IDIV_RATIO[7:0]	IDIV Register: frequency division ratio setting;
13	[15:8]	RESERVED	
	[7:0]	REG_MDIV_RATIO[7:0]	MDIV Register: frequency division ratio setting;
14	[15:14]	RESERVED	BANDWIDTH Register
	[13:12]	REG_VCTRL_INIT[1:0]	
	[11:10]	REG_CP_SELFBIAS_SEL[1:0]	
	[9:8]	REG_ICP_BASE_SEL[1:0]	
	[7:4]	REG_CP_CUR_SEL<3:0>	
	[3:1]	REG_LPF_R[2:0]	
	[0]	REG_LPF_C	
15	[15:6]	RESERVED	LOCK Register
	[5]	REG_LOCK_FILTER_PD	
	[4:0]	REG_FREQ_LOCKDET_SET<4:0>	

Detailed function description:

1. CLKOUT0 Register1

REG_ODIV0_RATIO is an integer frequency division ratio register, the configurable parameter range is 1~128, REG_ODIV0_DUTY is the output clock clkout0 duty ratio frequency ratio register, the configurable parameter range is 2~255, the duty ratio accuracy is 1/2N, N is Integer frequency division ratio, the range is 2/2N~(2N-1)/2N, according to the formula, when the duty ratio frequency ratio parameter is the same as the integer frequency division ratio parameter, the output duty cycle can be guaranteed to be 50%, so When configuring the output frequency, the duty cycle parameter should also be configured according to the requirements, such as the initial integer frequency division ratio and duty cycle are 24, when only the integer frequency division ratio parameter is changed to 15, the duty cycle parameter remains unchanged at 24, According to the formula, the output duty cycle is (24/2*15)*100%, which is 80%. At this time, the duty cycle frequency ratio needs to be configured as 15 to make the output duty cycle 50%.

In fractional frequency division, the duty ratio is not programmable, and the duty ratio frequency ratio needs to be configured to be the same as the integer frequency division ratio during configuration.

2. CLKOUT0 Register2

REG_ODIV0_FRACDIV_RATIO is the fractional frequency setting register for fractional frequency division, the parameter range is 1~7, and the precision is 0.125;

REG_ODIV0_FRACDIV_PSOFFSET is the fractional frequency division falling edge phase setting register, and

the parameter configuration is limited by REG_ODIV0_RATIO and REG_ODIV0_FRACDIV_PSOFFSET, as shown in Table 26;

REG_ODIV0_FPHASE is the phase fine adjustment setting register, see Chapter 2 Section 6.8 for details.

REG_ODIV0_CPHASE is the phase coarse adjustment register, see Chapter 2 Section 6.8 for details.

3. CLKOUT0 Register3

REG_ODIV0_ADJUST is the fractional frequency division timing adjustment setting, and the parameter configuration is limited by REG_ODIV0_RATIO and REG_ODIV0_FRACDIV_PSOFFSET, as shown in Table 26;

REG_ODIV0_FRACDIV_EN is the fractional frequency division enable signal. When configuring the fractional frequency division, the signal should be configured as 1, and configured as 0 to disable the fractional frequency division function;

REG_ODIV0_DPSORCAS_SEL is the VCO clock and interpolation phase shift clock selection, the parameter configuration is as follows:

2’b00: VCO clock, cooperate with REG_ODIV0_FPHASE to achieve fine adjustment, this parameter should be configured for phase fine adjustment;

2'b01: Interpolation phase shift clock;

2’b10: Input clock is 0;

2’b11: Input clock is 0.

REG_ODIV0_MUXSEL_EN is the output distributor input clock selection enable, configured as 1 is valid, configured as 0, the output clock is 0;

When configuring the fractional frequency division, the relevant parameters have a corresponding relationship, which must be configured strictly according to the corresponding relationship, otherwise the output frequency may be abnormal, as shown in the following table:

Table 26 Fractional frequency division parameter configuration list

REG_ODIV0_RATIO	REG_ODIV0_FRACDIV_RATIO	REG_ODIV0_FRACDIV_PSOFFSET	REG_ODIV0_ADJUST
Odd number	3’b001	3’b101	2’b00
	3’b010	3’b101	
	3’b011	3’b110	
	3’b100	3’b110	
	3’b101	3’b111	
	3’b110	3’b111	
	3’b111	3’b000	2’b01
Even	3’b001	3’b001	2’b11
	3’b010	3’b001	
	3’b011	3’b010	
	3’b100	3’b010	
	3’b101	3’b011	
	3’b110	3’b011	
	3’b111	3’b100	2’b10

4. CLKOUT1~ CLKOUT6 and CLKOUTF Register

5'h3~5'he are the register addresses of the output clock CLKOUT1~CLKOUT6. Compared with CLKOUT0, except that there is no fractional frequency division configuration, other parameter configuration methods are the

same; 5'hf~5'h11 are the feedback clock register addresses, and the parameter configuration method same as CLKOUT0.

5. IDIV Register

IDIV Register is the input frequency division register, the parameter range is 1~80.

6. MDIV Register

MDIV Register Feedback divider M frequency division ratio register, parameter range 1~128.

7. BANDWIDTH Register

BANDWIDTH Register is the loop bandwidth register, the specific parameters are as follows:

Table 27 GPLL BANDWIDTH Register parameter list

BANDWIDTH	PFD reference frequency range	Feedback divider	REG_CP_ SELFBIAS_SEL	REG_ICP_ BASE_SEL	REG_CP_ CUR_SEL	REG_ LPF_R	REG_ LPF_C
LOW OPTIMIZED	10<=F<=40MHz	15≤div＜20	1	0	3	7	0
		20≤div＜25			4		
		25≤div＜30			5		
		30≤div＜35			6		
		35≤div＜40			7		
		40≤div＜45			12		
		45≤div＜50			13		
		50≤div＜55			14		
		55≤div＜60			15		
		60≤div＜70		1	6		
		70≤div＜80			7		
		80≤div＜90			12		
		90≤div＜100			13		
		100≤div＜110			14		
		110≤div＜116			15		
		116≤div≤120		2	6		
HIGH	40<F<=450MHz	2≤div＜3	1	1	2	2	0
		3≤div＜4			3		
		4≤div＜5			4		
		5≤div＜6			5		
		6≤div＜7			6		

BANDWIDTH	PFD reference frequency range	Feedback divider	REG_CP_ SELFBIAS_SEL	REG_ICP_ BASE_SEL	REG_CP_ CUR_SEL	REG_ LPF_R	REG_ LPF_C
		7≤div<8			7		
		8≤div<9			12		
		9≤div<10			13		
		10≤div<11			14		
		11≤div<12			15		
		12≤div<14		2	6		
		14≤div<15			7		
		15≤div<16		3	5		
		16≤div<18		2	12		
		18≤div<20			13		
		20≤div<22			14		
		22≤div<24			15		
		24≤div<26		3	12		
		26≤div<29			13		
		29≤div≤32			14		
Remark			1: PFD reference frequency: CLKIN_FREQ/STATIC_RATIOI; 2: INTERNAL_FB is "CLKOUT0~6/F"; EXTERNAL_FB is "DISABLE"; Feedback divider = STATIC_RATIO0~6/F*STATIC_RATIOM; INTERNAL_FB is "DISABLE"; EXTERNAL_FB is "CLKOUT0~6/F"; Feedback divider = STATIC_RATIO0~6/F*STATIC_RATIOM;				

8. LOCK Register

REG_LOCK_FILTER_PD is the frequency lock detection glitch configuration control bit. When it is configured as 0, the LOCK output is filtered, and the LOCK signal will be pulled high after a delay of 320 feedback clock cycles. When it is configured as 1, the LOCK signal will be directly Output, the default configuration is 1.

REG_FREQ_LOCKDET_SET is the frequency lock precision configuration bit, it is recommended to configure the highest precision 5'b00000, and it is not recommended to configure other parameters.

5.3 Configuration restrictions

During dynamic configuration, there will be some constraints, including the above-mentioned configurable range, refer to Table 23, the input clock frequency range, VCO frequency range, and output frequency range are shown in Table 28 Operating frequency range.

Table 28 Operating frequency range

Parameter	Description	Minimum value	Typical value	Maximum value	Unit
FIN	Input clock frequency	10		800	MHz
FVCO	VCO operating frequency range	600		1200	MHz
FOUT	Output Clock Frequency Range	4.69		800	MHz

Note: Please refer to section 6.5 for calculation of FVCO and FOUT;

6. GTP_GPLL Function Description

6.1 Clock Input

When CLKIN_SEL is 0, select CLKIN1; when CLKIN_SEL is 1, select CLKIN2. The reference clock is dynamically switched between CLKIN1 and CLKIN2, and the PLL needs to be reset after switching. For the GPLL input clock, the following points should be noted:

- When the input clock is lost or unstable, the LOCK signal of the GPLL is pulled low, and the GPLL must be reset after recovery again.
- If there is no reference clock after power-on and power-on, the GPLL will output a low-frequency clock signal. At this time, the LOCK signal is low. If you want the output clock to be 0, you can use power-off mode or clock output gating. For details, see Sections 6.3 and 6.12.

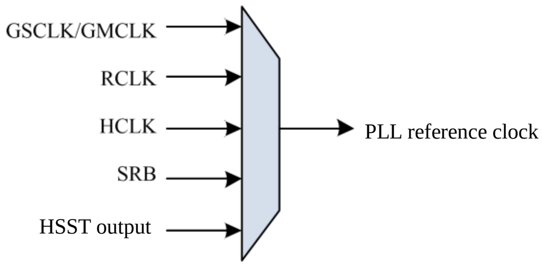


Figure 44 GTP_GPLL Reference Clock Source

6.2 GPLL reset

After the RST reset signal is released, the PLL starts to enter the lock state, and the PLL frequency lock is completed after the TLOCK time. The timing of the RST reset signal is shown in the figure below, and the high level is valid.

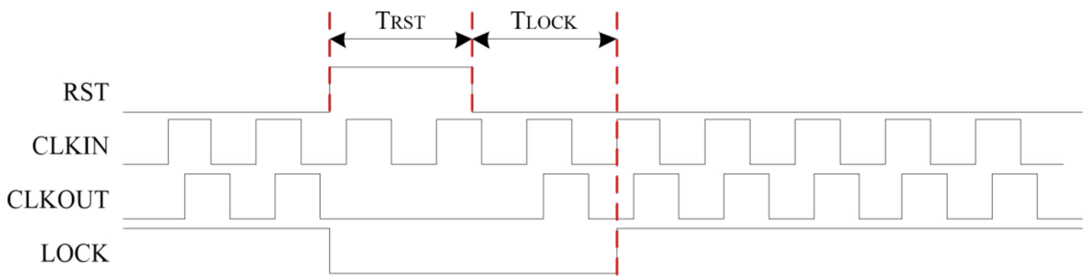


Figure 45 GTP_GPLL Reset Timing

The minimum pulse width of T_{RST} is 10ns, and the maximum lock time of T_{LOCK} is 200us.

6.3 GPLL power off

When PLL is not used, PLL_PWD=1, PLL can be turned off to save power.

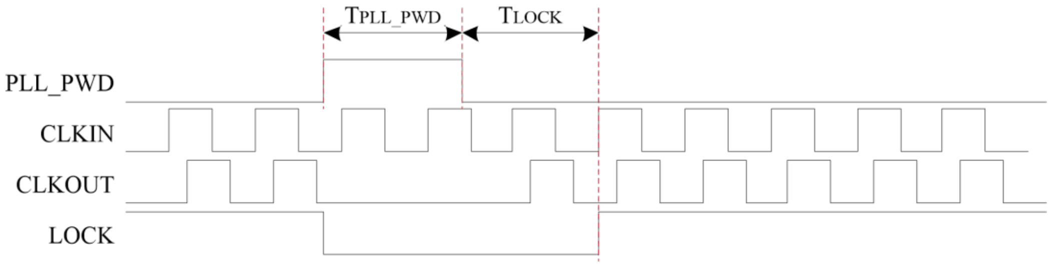


Figure 46 GTP_GPLL power-off sequence

T_{PLL_PWD} minimum pulse width 5ns, T_{LOCK} maximum lock time 200us.

6.4 Feedback Clock Selection

The feedback clock input source of GPLL can be divided into GPLL internal feedback and GPLL external feedback. The feedback source supports CLKOUT[0]~CLKOUT[6], CLKOUTF. By default, CLKOUTF is selected when internal feedback is selected, see section 8.1 for details.

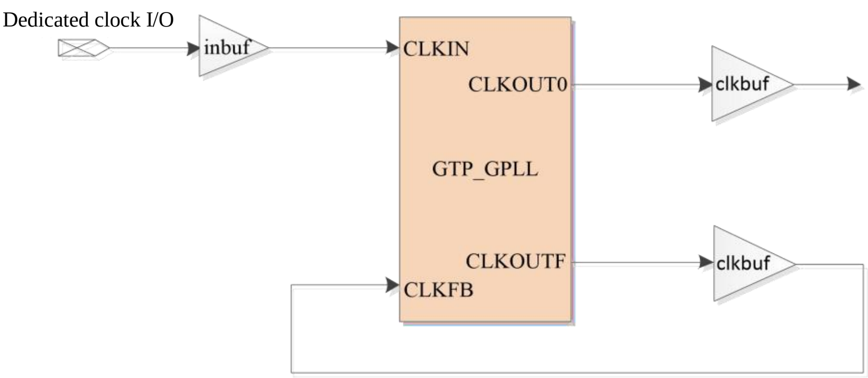


Figure 47 GTP_GPLL External Feedback Diagram

As shown in the figure, when external feedback is selected, the feedback clock reaches the feedback clock input through a dedicated clock path through the global clock or horizontal clock buffer, while in the internal feedback mode, the feedback clock output directly reaches the feedback clock input inside the PLL. little interference.

Table 29 Feedback Clock Selection

INTERNAL_FB	EXTERNAL_FB	Feedback mode
"CLKOUT0"	"DISABLE"	Internal feedback mode, select output divider0;
"CLKOUT1"	"DISABLE"	Internal feedback mode, select output divider1;
"CLKOUT2"	"DISABLE"	Internal feedback mode, select output divider2;
"CLKOUT3"	"DISABLE"	Internal feedback mode, select output divider3;
"CLKOUT4"	"DISABLE"	Internal feedback mode, select output divider4;
"CLKOUT5"	"DISABLE"	Internal feedback mode, select output divider5;
"CLKOUT6"	"DISABLE"	Internal feedback mode, select output divider6;
"CLKOUTF"	"DISABLE"	Internal feedback mode, select feedback F divider;
"DISABLE"	"CLKOUT0"	External feedback mode, select output divider0;
"DISABLE"	"CLKOUT1"	External feedback mode, select output divider1;
"DISABLE"	"CLKOUT2"	External feedback mode, select output divider2;
"DISABLE"	"CLKOUT3"	External feedback mode, select output divider3;
"DISABLE"	"CLKOUT4"	External feedback mode, select output divider4;
"DISABLE"	"CLKOUT5"	External feedback mode, select output divider5;
"DISABLE"	"CLKOUT6"	External feedback mode, select output divider6;
"DISABLE"	"CLKOUTF"	External feedback mode, select feedback F divider;

6.5 Output frequency programming

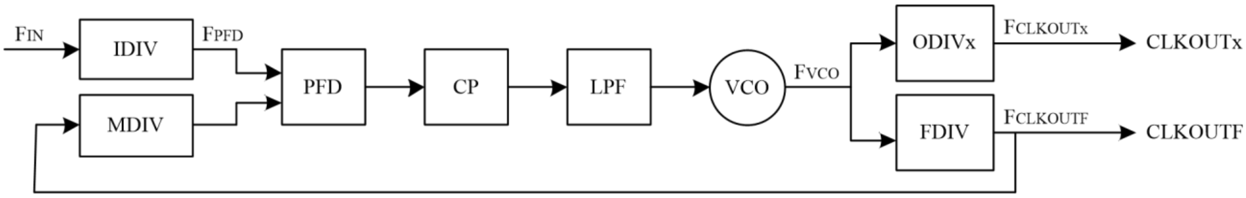


Figure 48 Schematic Diagram of GTP_GPLL Output Frequency Path

The reference clock (Fin) passes through the programmable input frequency divider (IDIV) to obtain a reference clock of the phase frequency detector (PFD), and the feedback clock passes through the programmable feedback frequency divider (FDIV) and (MDIV) to obtain the other 1 of the PFD A reference clock, PFD compares the phase and frequency of these two clocks, and then generates a signal to drive the charge pump (CP), the current signal generated by CP passes through the loop filter (LPF), and LPF generates a reference voltage for the voltage control Oscillator (VCO); PFD provides CP and LPF with phase leading or lagging signals to continuously adjust the frequency of VCO operation to adjust frequency and phase. For example, when VCO is still higher than the reference frequency after passing through the feedback frequency divider, PFD generates A downward adjustment signal makes CP and LPF reduce the voltage to control VCO to reduce the output frequency. When VCO is still lower than the reference frequency after passing through the feedback frequency divider, PFD generates an upward adjustment signal to make CP and LPF increase the voltage Control the VCO to increase the output frequency. The VCO generates 8-phase output clocks, and 1 channel of variable phase-shifted clocks can be generated through the 8-phase clocks, so as to realize phase shift coarse adjustment, phase fine adjustment and interpolation phase shift, and each output phase shift clock can be As the input of FDIV, there are 8 output frequency dividers, 7 ODIV and 1 FDIV, each frequency divider is independent, and the clock output by VCO passes through these frequency dividers to obtain the final output clock frequency.

Table 30 Description of output frequency programming parameters

No.	GTP parameters	Function name	Functional description
1	CLKIN_FREQ	F_{IN}	reference clock frequency;
2	STATIC_RATIOI	F_{PFD}	PFD input reference clock frequency is determined by the GTP parameter configuration frequency division coefficient in the list;
3	STATIC_RATIOF , STATIC_RATIOI, STATIC_RATIOM	F_{VCO}	The VCO output clock frequency is determined by the GTP parameter configuration frequency division coefficient in the list;
4	STATIC_RATIOF , STATIC_RATIOI, STATIC_RATIOM, STATIC_RATIO0~6	$F_{CLKOUTx}$	CLKOUTx output clock frequency is determined by the GTP parameter configuration frequency division coefficient in the list, x stands for 0~6;
5	STATIC_RATIOF	$F_{CLKOUTF}$	The CLKOUTF output clock frequency is determined by the GTP parameter configuration frequency division coefficient in the list;
6	STATIC_RATIOI	IDIV	Input frequency divider frequency division ratio;
7	STATIC_RATIOM	MDIV	Feedback Divider M Division Ratio
8	STATIC_RATIO0~6	ODIVx	Output frequency divider frequency division ratio, x represents 0~6;
9	STATIC_RATIOF	FDIV	Feedback divider F division ratio;

Note: CLKIN_FREQ is the default configuration parameter of the input clock frequency, not the input interface of the PLL. The input interface refers to Figure 39 CLKIN1, CLKIN2; the input and output frequency, PFD frequency range, etc. refer to the data sheet "DS05001".

If the frequency division ratio of the feedback frequency divider selected by internal feedback or external feedback is FBDIV, the calculation formula of each clock frequency in Figure 48 is as follows:

$$F_{PFD} = \frac{F_{IN}}{IDIV}$$

$$F_{VCO} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV}$$

$$F_{CLKOUTx} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV \times ODIVx}$$

$$F_{CLKFBOUT} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV \times FDIV}$$

Among them, FBDIV is the frequency division ratio of the frequency divider selected by the feedback loop, FBDIV∈[ODIV0~6,FDIV], for example, when the feedback clock is CLKOUT0, FBDIV=ODIV0.

The output clocks CLKOUT0 and CLKOUTF not only support integer frequency division mode, but also support fractional frequency division mode.

(1) ODIV0 frequency division ratio

ODIV0 = CLKOUT0 integer frequency division ratio + CLKOUT0 fractional frequency division ratio

The frequency division ratio corresponding to ODIV0 corresponds to the value of parameter STATIC_RATIO0.

(2) FDIV division ratio

FDIV = CLKOUTF integer frequency division ratio + CLKOUTF fractional frequency division ratio

The frequency division ratio of FDIV corresponds to the value of parameter STATIC_RATIOF.

6.6 Loop Bandwidth

The GPLL loop bandwidth can be configured as low bandwidth (LOW), medium bandwidth (OPTIMIZED) and high bandwidth (HIGH). The parameters of low bandwidth and medium bandwidth configuration are the same, see Table 27 for details.

Considering that the input clock is not an ideal clock in practical applications, different bandwidth configurations have different effects on the PLL:

(1) If the PLL output clock is expected to have a small Jitter, configure it as low bandwidth or medium bandwidth, and the locking time is long at this time;

(2) If the PLL lock time is expected to be short, configure it as high bandwidth, and the output clock Jitter will become worse at this time;

6.7 Fractional frequency division

ODIV0 (STATIC_RATIO0) and FDIV (STATIC_RATIOF) support both integer frequency division and fractional frequency division modes.

(1) Fractional frequency division precision 0.125;

(2) Fractional frequency division mode does not support interpolation phase shift and dynamic phase shift mode of static phase shift mode;

(3) The duty cycle of the fractional frequency division mode is not programmable; if the integer part of the fractional frequency division is N, and the fractional part is f, the calculation formula of the duty cycle is as follows:

$$DutyCycle = 50\% + \frac{\alpha}{2(8N + \frac{f}{0.125})}$$

where $\frac{f}{0.125} = odd, \alpha = 1, \frac{f}{0.125} = even, \alpha = 0;$

Example: ODIV0 STATIC VALUE=24 for the integer part of the frequency division coefficient, ODIV0 Fraction VALUE=1/8 for the fractional part of the frequency division coefficient can be obtained as N=24, f=0.125, α=1, DutyCycle = 50%+1/2(8 *24+1)=50.259%.

Only the output clocks CLKOUT0 and CLKOUTF support fractional frequency division. The fractional frequency division configuration of CLKOUT0 is realized by configuring the parameter STATIC_RATIO0, and the fractional frequency division configuration of CLKOUTF is realized by configuring the parameter STATIC_RATIOF. If you want the frequency division ratio of CLKOUT0 to be 2.125, set the parameter The value of STATIC_RATIO0 can be configured as 2.125, and the configuration method of CLKOUTF is the same. It should be noted that the output clock frequency must be within the configurable range, refer to Table 28.

6.8 Phase adjustment

Phase adjustment includes three methods: coarse phase adjustment, fine phase adjustment and interpolation phase shift. The coarse phase adjustment and fine phase adjustment have both static configuration mode and adjustment through the APB interface. These two adjustment methods are independent of each clock output; and The interpolation phase shift can be statically configured or adjusted through the dynamic configuration interface DPS interface, which will affect all output clocks that select this mode. The output clock as a feedback clock cannot be phase adjusted.

(1) Phase adjustment method:

➢ Phase coarse adjustment

By configuring the parameter STATIC_CPHASE0/1/2/3/4/5/6/F, the phase of the output clock CLKOUT0/1/2/3/4/5/6/F can be roughly adjusted, and the parameter configuration range can be referred to Table 23.

Relative to the input VCO clock, the output clock CLKOUT0/1/2/3/4/5/6/F phase coarse adjustment adjustment time step is Tvco, the adjustment range is [0~Ndiv-1]*Tvco, the adjustment degree step The order is 360°/Ndiv.

Ndiv is the output frequency division ratio ODIVx and the feedback frequency division ratio FDIV. For example, the frequency division coefficient Ndiv of the output clock CLKOUT0 is 6. According to the formula, the degree of each adjustment is 60°, and the parameter configuration takes an integer multiple of Ndiv as a cycle. When Ndiv is 6, the corresponding relationship between CLKOUT0 and STATIC_CPHASE0 is as follows:

STATIC_CPHASE0=0, CLKOUT0 phase shift 0°;

STATIC_CPHASE0=1, CLKOUT0 phase shift 60°;

STATIC_CPHASE0=2, CLKOUT0 phase shift 120°;

STATIC_CPHASE0=3, CLKOUT0 phase shift 180°;

STATIC_CPHASE0=4, CLKOUT0 phase shift 240°;

STATIC_CPHASE0=5, CLKOUT0 phase shift 300°;

STATIC_CPHASE0=6,CLKOUT0 phase shift 0°.

➢ Phase fine adjustment

By configuring the parameter STATIC_PHASE0/1/2/3/4/5/6/F, the phase fine adjustment of the output clock CLKOUT0/1/2/3/4/5/6/F can be realized, and the parameter configuration range can be referred to Table 23.

Relative to the input VCO clock, the output clock CLKOUT0/1/2/3/4/5/6/F phase fine adjustment adjustment time step is Tvco, the adjustment range is (0~7/8) Tvco, the adjustment degree step It is 45°/Ndiv, and the adjustment range is (0°~45°*7)/Ndiv.

For example, the VCO frequency is 1000MHz, and the output frequency division factor of CLKOUT0 is 24. According to the formula, the time of each adjustment is 125ps, and the adjustment range is 0ps~875ps; the degree of each adjustment is 1.875°, and the adjustment range is 0°~13.125°.

STATIC_CPHASE0=0, the corresponding relationship between CLKOUT0 configurable phase and STATIC_PHASE0 is as follows:

STATIC_PHASE0=0, CLKOUT0 phase shift 0°

STATIC_PHASE0=1, CLKOUT0 phase shift 1.875°;

STATIC_PHASE0=2, CLKOUT0 phase shift 3.750°;

STATIC_PHASE0=3, CLKOUT0 phase shift 5.625°;

STATIC_PHASE0=4, CLKOUT0 phase shift 7.50 0°;

STATIC_PHASE0 =5, CLKOUT0 phase shift is 9.375°;

STATIC_PHASE0=6, CLKOUT0 phase shift is 11.250°; S

TATIC_PHASE0=7, CLKOUT0 phase shift is 13.125°.

➢ Interpolation phase shift

The static interpolation phase shift of CLKOUT0/1/2/3/4/5/6/F can be realized by configuring the parameter STATIC_PHASE and the enable signal CLK_DPS0/1/2/3/4/5/6/F_EN, shared by all output clocks for parameter STATIC_PHASE, refer to Table 23 for the configurable range. If you need to configure the CLKOUT0 static interpolation phase shift function, you need to configure CLK_DPS0 _EN as "TRUE" and set the value of STATIC_PHASE.

Through the enable signal CLK_DPS0/1/2/3/4/5/6/F_EN and the DPS port, the dynamic interpolation phase shift function of CLKOUT0/1/2/3/4/5/6/F can be realized, and all output clocks share 1 DPS interface, if you need to configure the CLKOUT0 static interpolation phase shift function, you need to configure CLK_DPS0 _EN as "TRUE", and then dynamically adjust the CLKOUT0 output clock phase through the DPS interface.

Relative to the input VCO clock, the output CLKOUT0/1/2/3/4/5/6/F interpolation phase shift accuracy Tvco/64, the adjustment degree step is 360°/(64*Ndiv).

Dynamic phase modulation adopts interpolation Phase shift, the output clock can achieve 360-degree circular rotation, see "Dynamic Adjustment" in this section for details.

The adjustment range of the static interpolation phase shift degree is (0~63)* 360°/(64*Ndiv).

For example, the VCO frequency is 1000MHz, and the output frequency division factor of CLKOUT0 is 24. According to the formula, the time of each adjustment is 15.625ps, and the degree of each adjustment is 0.234575°. The maximum value of static interpolation phase shift adjustment is 14.765625°, 1 VCO clock cycle; since the output clock is obtained by dividing VCO by Ndiv, the dynamic interpolation phase shift realizes a 360° adjustment after 24 VCO clock cycles, and the total number of adjustments is 64*24.

Note:

- Ndiv∈{STATIC_RATIO0~6, STATIC_RATIOF}, is the frequency division coefficient of the output clock CLKOUT0/1/2/3/4/5/6/F, and the parameter configurable range refers to the GTP_GPLL parameter list.

- In the process of phase adjustment, only one of phase fine adjustment and interpolation phase shift can be selected to cooperate with phase coarse adjustment to realize output clock phase adjustment.

(2) Phase adjustment mode:

➢ Static configuration

The output clock CLKOUT0/1/2/3/4/5/6/F phase fine-tuning static configuration is controlled by STATIC_PHASE0/1/2/3/4/5/6/F respectively;

The output clock CLKOUT0/1/2/3/4/5/6/F Phase coarse static configuration is controlled by STATIC_CPHASE0/1/2/3/4/5/6/F respectively;

Output clock CLKOUT0/1/2/3/4/5/6/F interpolation Phase shift static configuration is controlled by STATIC_PHASE;

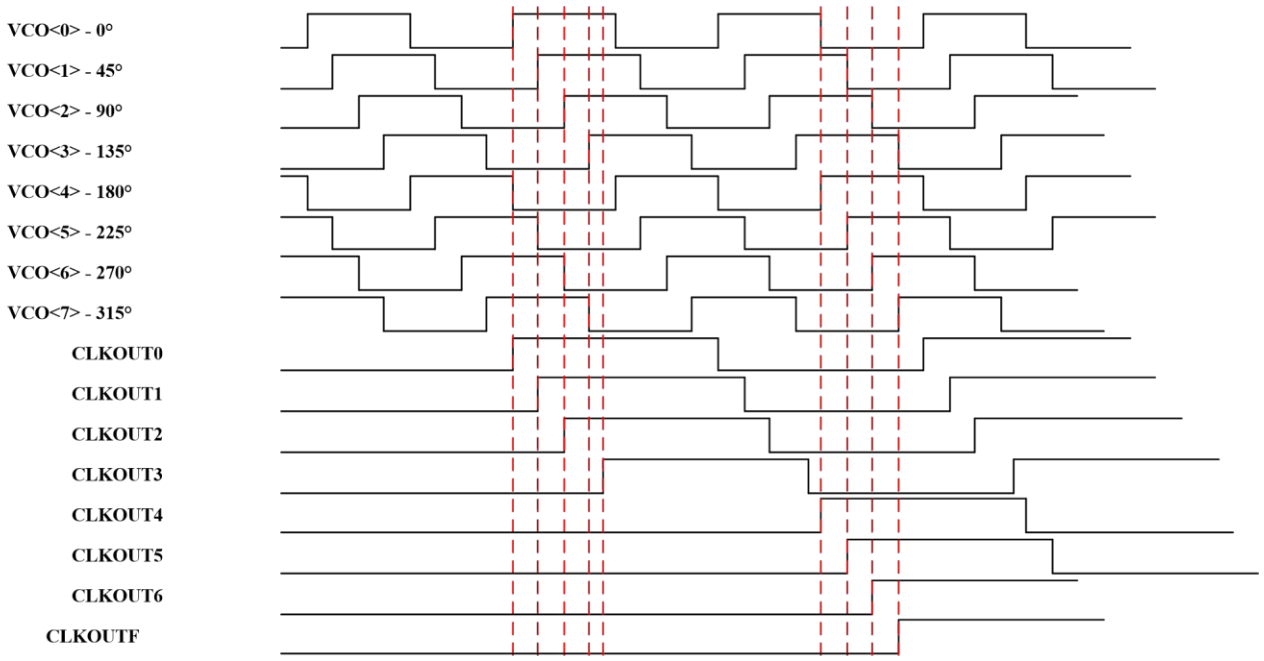


Figure 49 GTP_GPLL phase adjustment_static configuration

As shown in the table below, CLKOUT0 is generated by VCO<0> divided by 2, the phase of fine adjustment is 0, and the phase of coarse adjustment is 0. Taking CLKOUT0 as the reference, the phase relationship of each output clock is as follows:

Note: According to the formula, since ODIV0=2, the minimum fine-tuning phase step=45°/2=22.5°, the minimum coarse-tuning phase step=180°, and the minimum interpolation phase shift step=2.8125°.

Table 31 Output Clock Phase Relationship

Output clock	Fine tune phase	Coarse phase	Interpolation phase shift	Phase relationship
CLKOUT0	0	0	---	0
CLKOUT1	1*Tvco/8	0	---	22.5°
CLKOUT2	2*Tvco/8	0	---	45°
CLKOUT3	0	0	28*Tvco/64	78.75°
CLKOUT4	4*Tvco/8	Tvco	---	270°
CLKOUT5	5*Tvco/8	Tvco	---	292.5°
CLKOUT6	6*Tvco/8	Tvco	---	315°
CLKOUTF	7*Tvco/8	Tvco	---	337.5°

➢ Dynamic adjustment

The GTP_GPLL module of PG2T390H supports the interface of dynamic phase adjustment and dynamic phase shift adjustment. Dynamic phase adjustment allows the phase of the PLL output clock to be dynamically adjusted

relative to the reference clock. The dynamic phase adjustment function is realized through four signals DPS_CLK, DPS_EN, DPS_DIR and DPS_DONE. The phase can be increased or decreased by setting DPS_DIR. Every adjustment, the phase of the GPLL output clock changes by 1/64*Tvco. There is no maximum value for phase adjustment, and any clock frequency can achieve 360° phase adjustment. When a cycle ends, the phase adjustment cycle starts again.

The dynamic phase adjustment process is shown in the figure below. DPS_EN, DPS_DIR and DPS_DONE are synchronized to the DPS_CLK clock domain. When DPS_EN is high (one DPS_CLK clock cycle), the phase adjustment is initialized. When DPS_DIR is low, the phase is increased, and DPS_DIR is high. When the level is low, the phase is reduced. When the phase adjustment is completed, DPS_DONE lasts for 1 DPS_CLK cycle high level. The entire adjustment process lasts for 15 clock cycles.

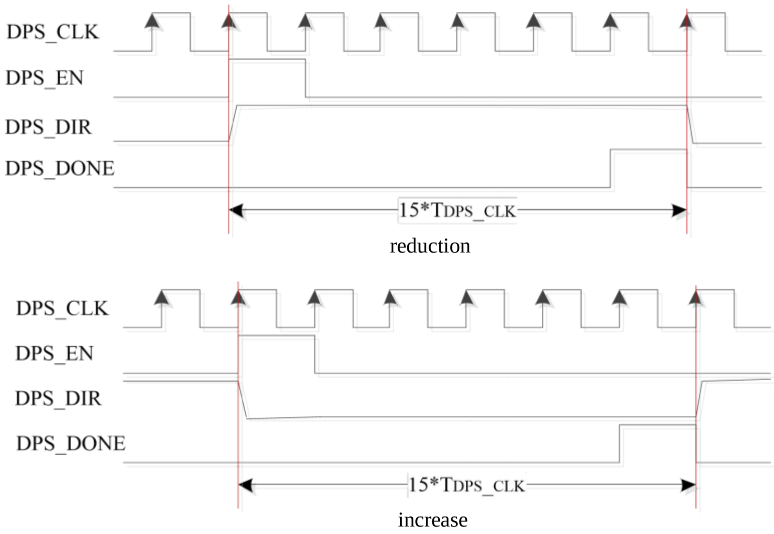


Figure 50 GTP_GPLL dynamic phase shift mode interface timing table

The dynamic phase shift interface is shown in the table below,

Table 32 Dynamic phase shift port description

Serial number	Port name	I/O	Description	Initial value
1	DPS_CLK	I	Dynamic phase adjustment of the clock signal; FMAX = 500MHz;	
2	DPS_EN	I	Dynamic phase adjustment enable signal;	
3	DPS_DIR	I	Dynamic phase adjustment directional control; 1’b0: Increase, 1’b1: Decrease;	
4	DPS_DONE	O	Dynamic phase adjustment completion indication signal;	1’b0

6.9 Programmable Duty Cycle

The output divider supports programmable Duty Cycle, the minimum step is 50%/odiv, and odiv is the frequency division coefficient of the output clock divider. STATIC_DUTY0/1/2/3/4/5/6/F determines the duty cycle after frequency division, expressing The formula is as follows, duty is the configuration value of duty cycle. duty cycle = (50%/odiv)*duty.

For example, if odiv is 24, then according to the formula, the range of duty can be 2~47, and the range of duty cycle is 4.17%~97.92%.

Note: (1) The setting value of DUTY is limited by the odiv value (output frequency division):

odiv >1,2=< duty <= 2* odiv -1;

odiv =1, duty is invalid, does not work, the default is 50% output.

(2) Fractional frequency division does not support duty cycle programming;

6.10 Spread Spectrum Clock Generation and Input

- Support spectrum spread clock input, the modulation frequency is less than GPLL bandwidth;
- Support local spread spectrum clock generation, support center spread spectrum and down spread spectrum two modes;
- Center spread HIGH max ±2%, center spread LOW max ±1%, down spread HIGH max -2%; down spread LOW max -1%

The center spread spectrum is shown in the figure below, where the black solid line represents the high-center spread spectrum modulation, and the blue solid line represents the low-center spread spectrum modulation.

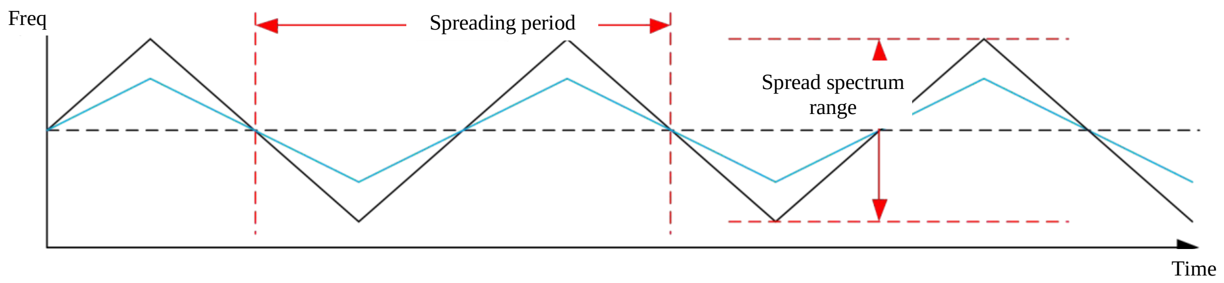


Figure 51 Schematic diagram of GPLL center spread spectrum

Down-spreading is shown in the figure below, where the black solid line represents high-down-spreading modulation, and the blue solid line represents low-down-spreading modulation.

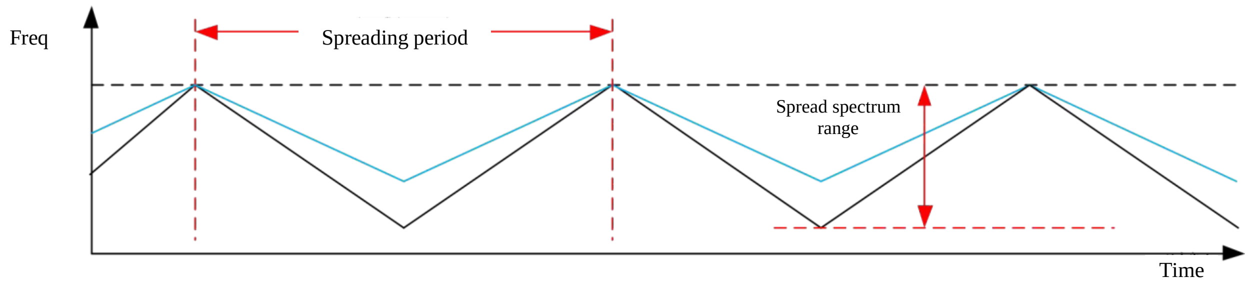


Figure 52 Schematic diagram of GPLL down-spreading

When GPLL works in SSC mode, it needs to use the original clock resource to generate spread spectrum clock, so:

(1) CLKOUT2/N and CLKOUT3/N are no longer used independently;

(2) The dynamic phase shift mode is no longer used;

6.11 Clock output cascading

When CLK_CAS5_EN is configured as "TRUE", output divider5 and output divider6 can realize clock cascading.

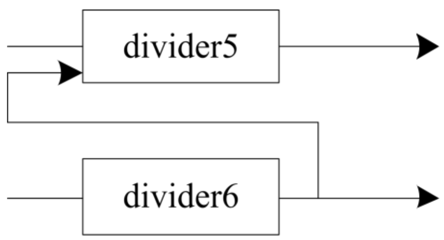


Figure 53 GTP_GPLL OUTPUT Divider Output Cascading

After cascading, the output clock CLKOUT5 has a fixed phase deviation with other output clocks.

6.12 Clock output gating

The GTP_GPLL input signal CLKOUT0_SYN is used to enable and disable the CLKOUT0 output clock. When the user does not need the CLKOUT0 clock, the clock can be turned off to save Clock Tree and Fabric power consumption.

CLKOUT0_SYN signal is optional, when the user configures CLKOUT0_SYN_EN as "TRUE", the signal is valid.

Similarly, the input signal CLKOUT1~6/F_SYN cooperates with the configuration bit CLKOUT1~6/F_SYN_EN to enable and disable the CLKOUT1~6/F clock.

Taking the output clock CLKOUT0 as an example, the functional diagram is shown in the figure below.

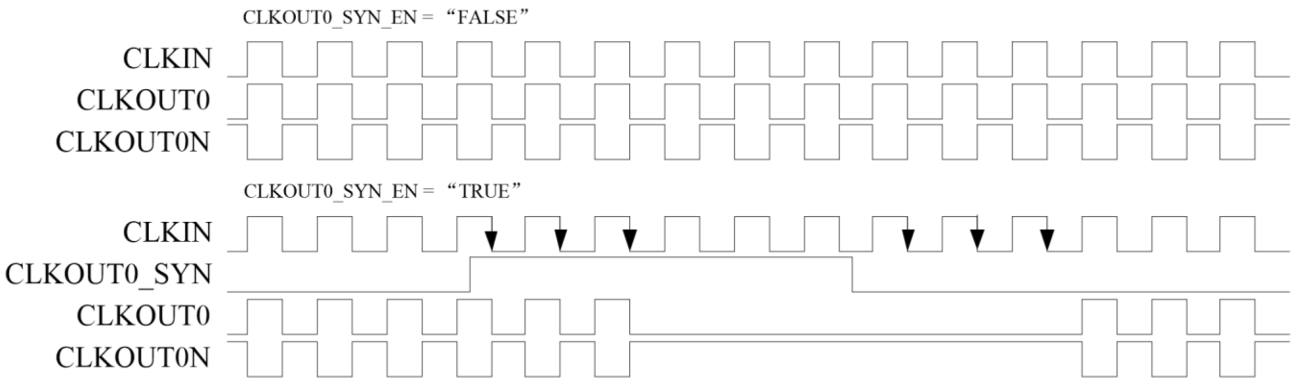


Figure 54 GTP_GPLL output clock GATE timing diagram

6.13 LOCK indication

GPLL supports two LOCK modes, which are selected by the configuration parameter LOCK_MODE.

Table 33 GPLL LOCK indication modes

Parameter name	Parameter value	Functional description
LOCK_MODE	0	Monitor the state of PLL LOCK in real time, once it enters an abnormal state, it will pull down LOCK
	1	LOCK will not monitor (indicate) the PLL working status in real time; once LOCK 1 is pulled high, it will not be pulled low unless it is reset or Power Down

7. GTP_GPLL configuration constraints

In practical applications, relevant parameters need to be configured to realize certain functions, and the configurable ranges of these parameters affect each other. It is configurable within the entire range of the GPLL. If the parameters are misconfigured, it may cause the GPLL to work abnormally. Therefore, it is necessary to know the restrictions and configurable range of the relevant parameters when configuring.

There are two ways to configure GPLL, one is through GUI (IP compiler in PDS tool), for the usage method of this configuration, please refer to "UG041001", which can be found in the IP configuration interface; the other way is to instantiate the original language, and then configure the relevant parameters according to the specific realized functions, you can combine the GPLL Advanced mode in the IP compiler to understand the configuration constraints, for example, if some parameters are set in the wrong range, an error will be reported when the IP is generated, and the configurable range will also be reminded.

Please refer to Table 23 and Table 28 for the configurable range of parameters.

1. Output clock frequency constraints

One of the most commonly used functions of the GPLL is to configure the desired output frequency. The following factors need to be considered:

- The selected input frequency must be within the configurable range;
- The output clock frequency must be within the configurable range;
- PFD frequency must be within the configurable range;
- Input frequency division parameters IDIV, output frequency division parameters ODIV, feedback frequency division parameters MDIV, FBDIV must be within the configurable range;
- VCO frequency range must be within the specified range.

If the desired output clock frequency is 100MHz, the input clock frequency is selected to be 50MHz;

First consider the PFD frequency. According to the formula, since the input clock is 50MHz, the PFD frequency range is 10MHz to 450MHz, so the IDIV can be configured from 1 to 5. If you choose 1, select the internal feedback mode, and the feedback output clock frequency is 50MHz. The clock frequency is the same, at this time FBDIV=FDIV, according to the formula, MDIV=1.

Parameters determined by the above two steps: CLKIN1=50MHz, PFD frequency=50MHz, CLKOUT0=100MHz, IDIV=MDIV=1.

Then according to the VCO formula and the VCO frequency range, the configurable range of FBDIV is 12 to 24. If you choose 24 (try to make the VCO work at the highest frequency), then according to the output clock frequency formula, you can get ODIV0=6, and the VCO frequency is 1200MHz.

Through the above steps, we get an effective output clock frequency.

The related formula is as follows:

- PFD frequency calculation formula: $F_{PFD} = \frac{F_{IN}}{IDIV}$
- VOC frequency calculation formula: $F_{VCO} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV}$
- Output clock CLKOUT0~6 frequency calculation formula: $F_{CLKOUTx} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV \times ODIVx}$
- Feedback clock output frequency calculation formula: $F_{CLKFBOUT} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV \times FDIV}$

2. Duty Cycle Constraints

Please refer to Section 6.9 Duty Cycle Programmable in this chapter.

3. Phase adjustment constraints

Please refer to Section 6.8 Phase Adjustment in this chapter.

8. GTP_GPLL application mode

8.1 Internal Feedback Mode

The internal feedback mode is mainly for certain application scenarios, which have high performance requirements for the GPLL output clock, such as frequency synthesis, low jitter clock output, etc.

In the internal feedback mode, the feedback clock is directly connected to the input of the GPLL without passing through any other circuits, thus avoiding the noise introduced by other circuits and having better jitter performance.

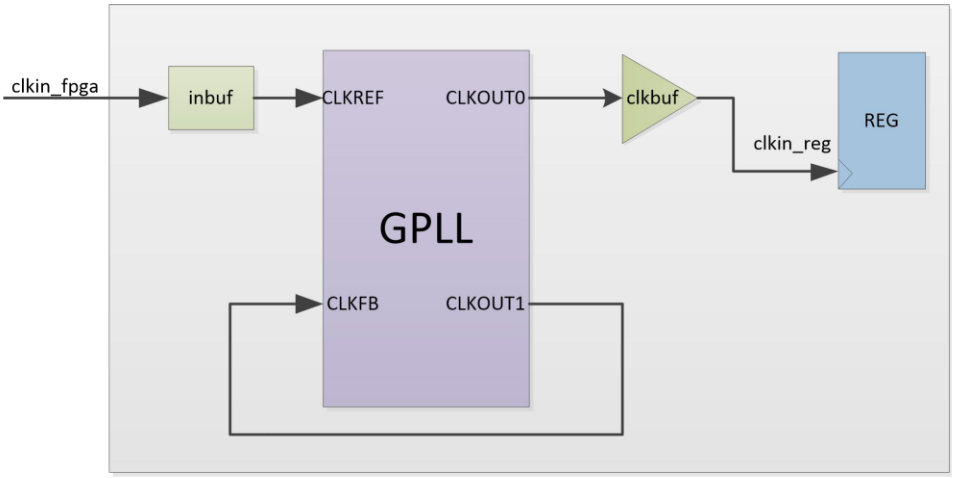


Figure 55 Schematic Diagram of GPLL Internal Feedback Mode

8.2 Source synchronous mode

Use external feedback to realize the source synchronous mode. The source synchronous mode is mainly for the GPLL output clock to drive the internal register. It is necessary to ensure that the input clock and the data maintain a certain phase relationship, as shown in the figure below. When the GPLL is locked, the phase of the b/e point is Aligned, in source synchronous mode, the path of the GPLL output clock clkout0 to the register and the path experienced by the feedback clock clkout1 must be symmetrically balanced, and use the same 1regional buffer, that is, to ensure that the clock phases of point c and point e are aligned, that is, b Point c is aligned with the clock phase of point c; at the same time, the skew (offset) between the data pin to the register data terminal input and the clock pin to the GPLL input reference clock can be compensated through the GPLL phase adjustment function, that is, point d to point f and The offset from point a to point b, so that the phase edge or center alignment between data and clock can be realized at the internal REG of FGPA, specifically 0° or 90° alignment, depending on the user's requirements, the specific phase shift requirements It can be realized by the phase shift function of the frequency divider of the output clock.

For example, when the rising edge of the input pin clock enters the FPGA at the center of the data, the GPLL output phase shift function can be used to move the phase of clkout0, and the internal register of the FPGA can realize the rising edge of the clock is aligned with the center of the data. At this time, if the input If there is no skew between the reference input of the clock clkin_fpga entering the GPLL and data entering the register, such as taking a dedicated clock path, that is, the skew is very small. At this time, the GPLL can automatically realize the above-mentioned clock rising edge and data center without any phase shift adjustment. Center aligned.

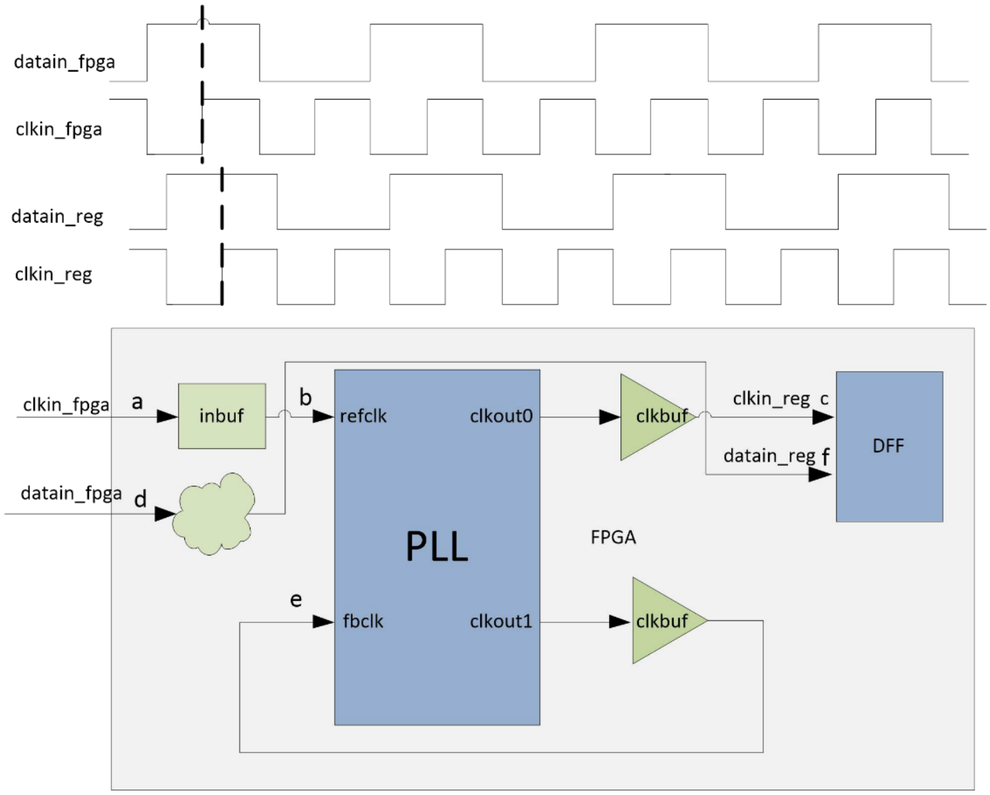


Figure 56 Schematic Diagram of GPLL Source Synchronous Mode

8.3 Zero Latency Mode

Using external pin feedback to achieve zero-delay mode is mainly for the case where there is only one input reference clock and the FPGA drives multiple external devices. It is necessary to ensure that the input clock of the external device is aligned with the clock of the FPGA input pin, as shown in the figure below Show.

In zero-delay mode, the input clock and the feedback clock need to use the same IO standard to ensure that point a and point d are phase aligned, and point b and point e are phase aligned. At the same time, the feedback clock trace on the board and the clock trace driving the external device If they match each other and are equal in length, the phases of the clocks at points d and c are aligned, so the clocks at points a and c are aligned to realize the function of zero-delay buffering.

In actual situations, due to the inconsistency between the load parasitic capacitance of the external device and the parasitic capacitance of the FPGA input pin, the timing of the rising or falling edge of the signal at point c and point d will be inconsistent, resulting in a slight difference in delay. Therefore The difference in skew of the a/c clock, the customer needs to take it into account when the timing is converged, leaving a certain margin.

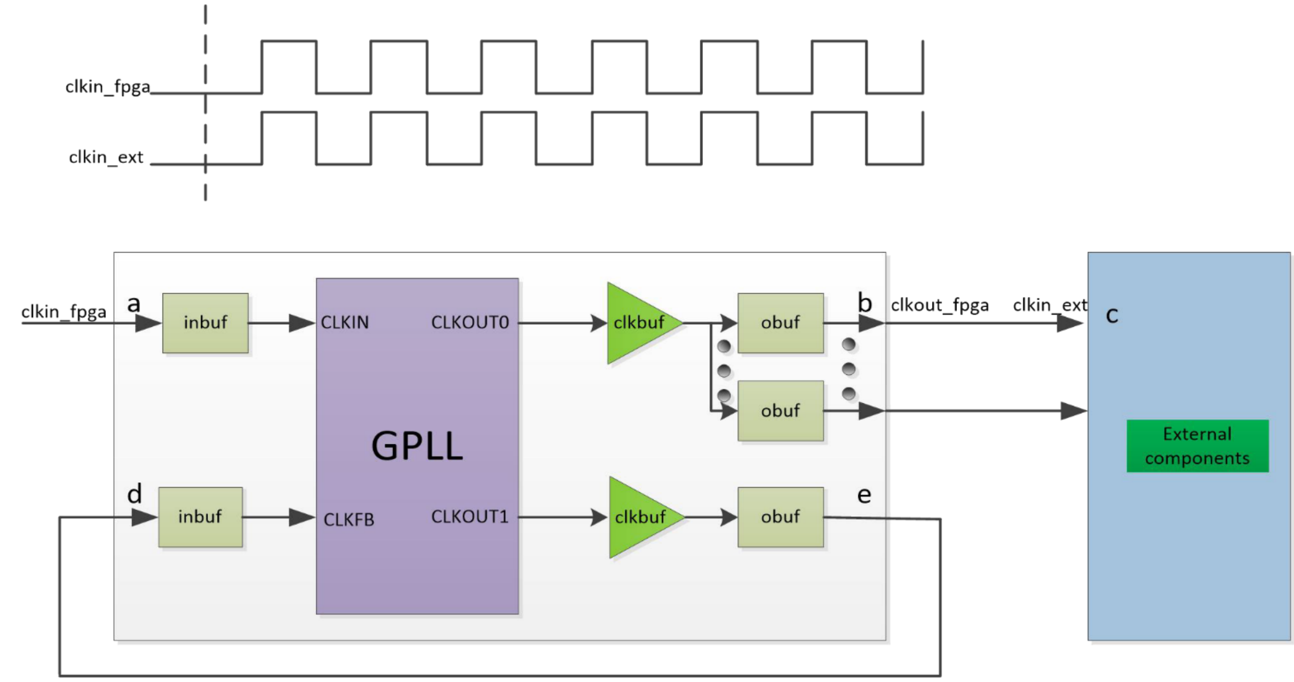


Figure 57 Schematic Diagram of GPLL Zero Latency Mode

8.4 Cascading between GPLLs

GPLLs can be cascaded, and the output interface CLKOUT0~3 is connected to the input reference clock terminal through the PLL clock tree. The frequency selectivity obtained by cascading each other is more. For example, the external input clock frequency is 20MHz. By cascading the first-level GPLL Output a 50MHz clock as the input of the second-stage GPLL. According to the output frequency calculation formula, the effective output clock frequencies obtained by these two frequencies are different. There is a phase offset between the output clocks of the two GPLLs.

The output frequency cascade formula is as follows:

Cascade output frequency formula: $F_{CLKOUTx} = (\frac{F_{IN} \times MDIV \times FBDIV}{IDIV \times ODIVx})(GPLL1) \times (\frac{MDIV \times FBDIV}{IDIV \times ODIVx})(GPLL2)$

As shown in the following two cascading block diagrams:

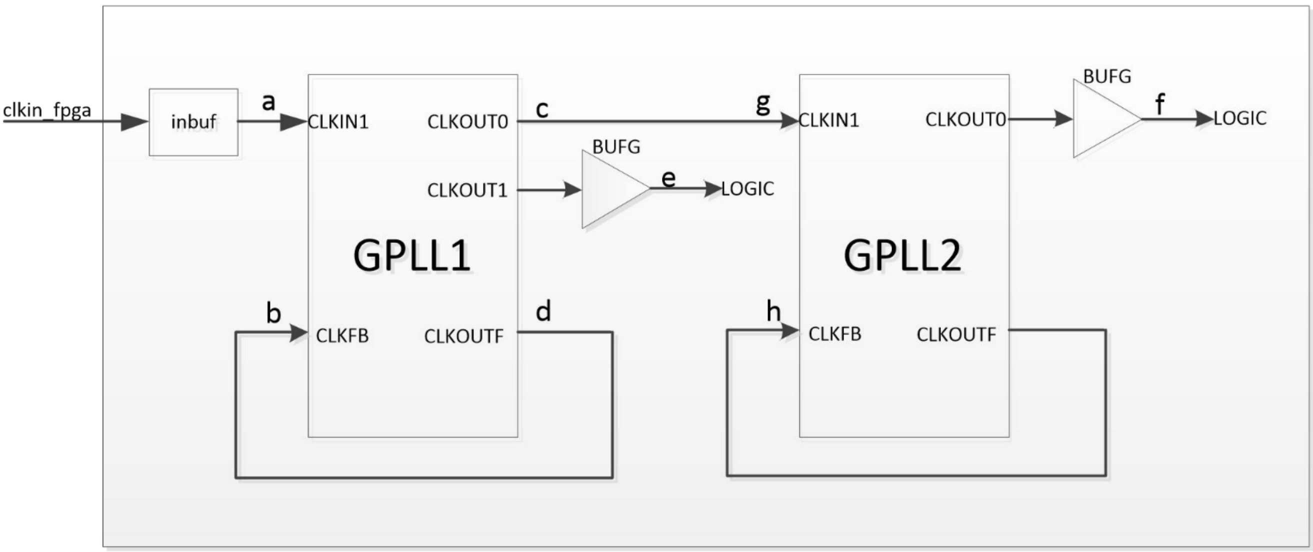


Figure 58 Two GPLL cascaded mode 1

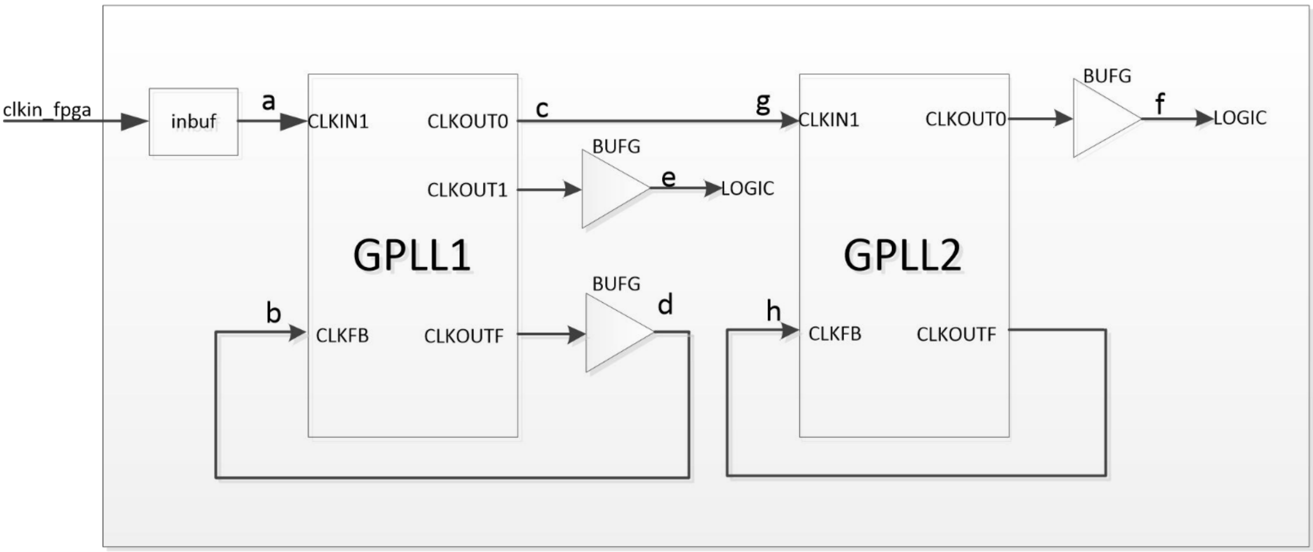


Figure 59 Two GPLL cascaded mode 2

Note: GPLL and PPLL can be cascaded.

(3) PPLL instructions

1. PPLL overview

PPLL is the core subsystem for FPGA to provide clock resources. There are 10 PPLL modules inside PG2T390H. The specific resources are shown in the red circle in the figure below. PPLL mainly provides for FPGA: clock frequency synthesis, clock skew reduction (skew), phase adjustment, output Clock Gate and APB dynamic reconfiguration and other functions.

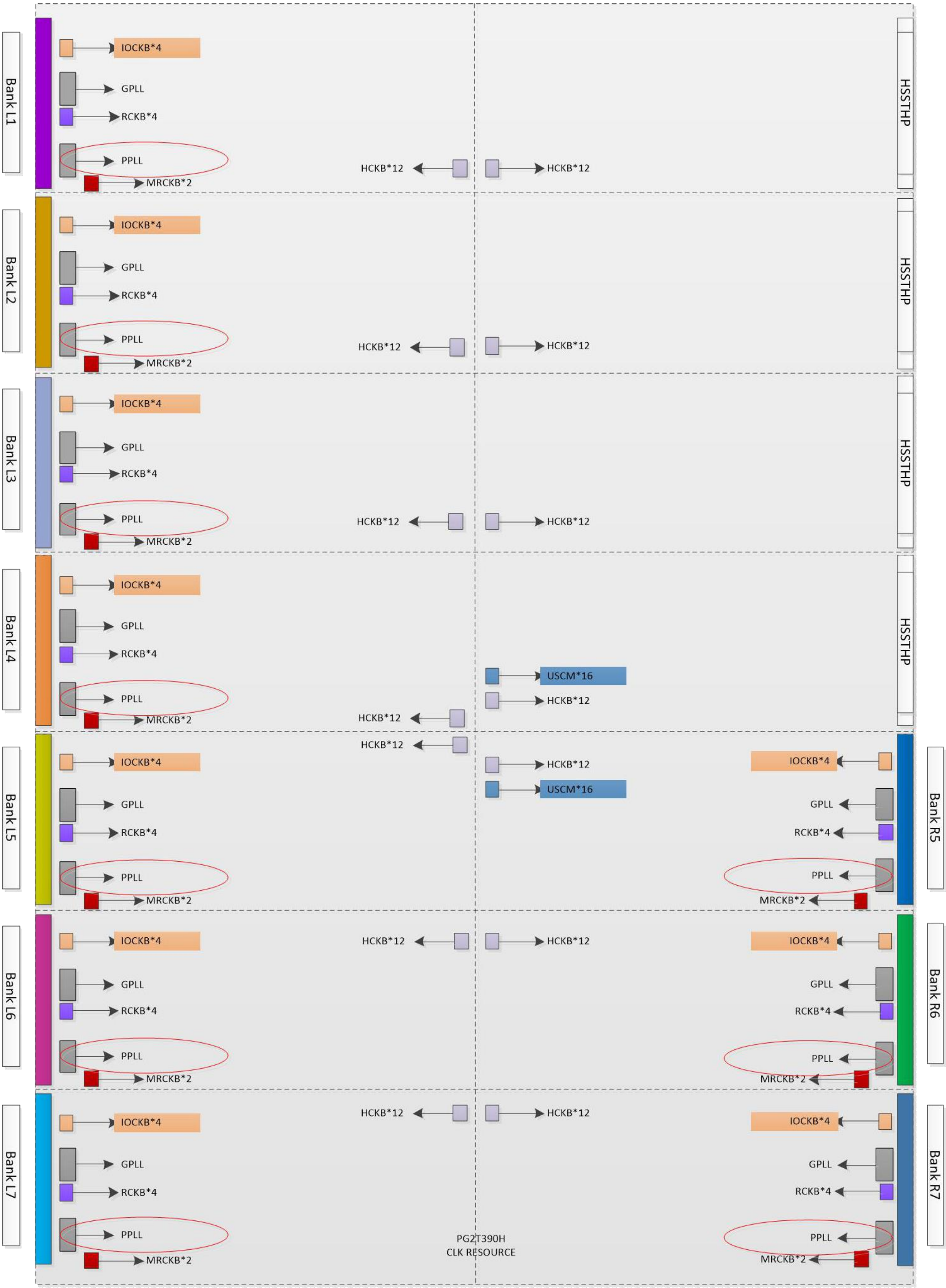


Figure 60 PPLL Resource Diagram

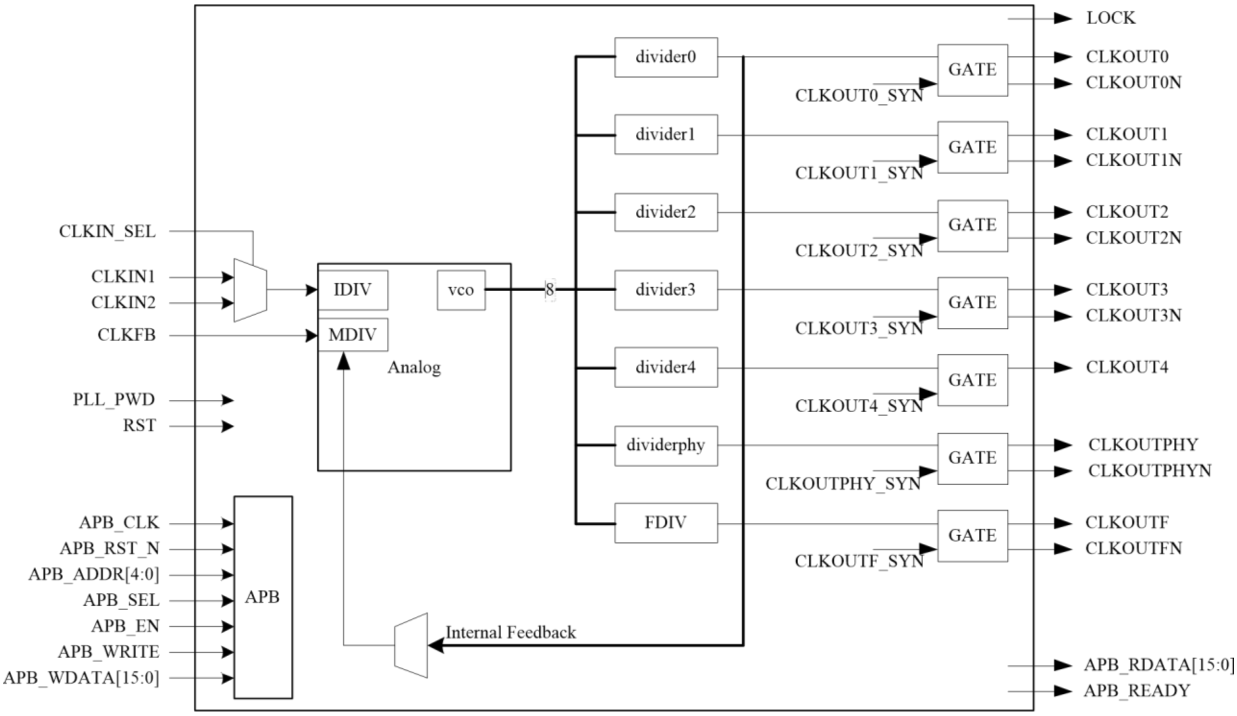


Figure 61 PPLL System Block Diagram

In use, it is configured by calling the GTP_PPLL instance. For unused clock output ports, the output shutdown can be configured to reduce power consumption. The clock output of CLKOUTPHY in GTP_PPLL is dedicated to the clock of DDR PHY, and the user logic should not be used. The application of GTP_PPLL is introduced below.

2. GTP_PPLL top-level block diagram

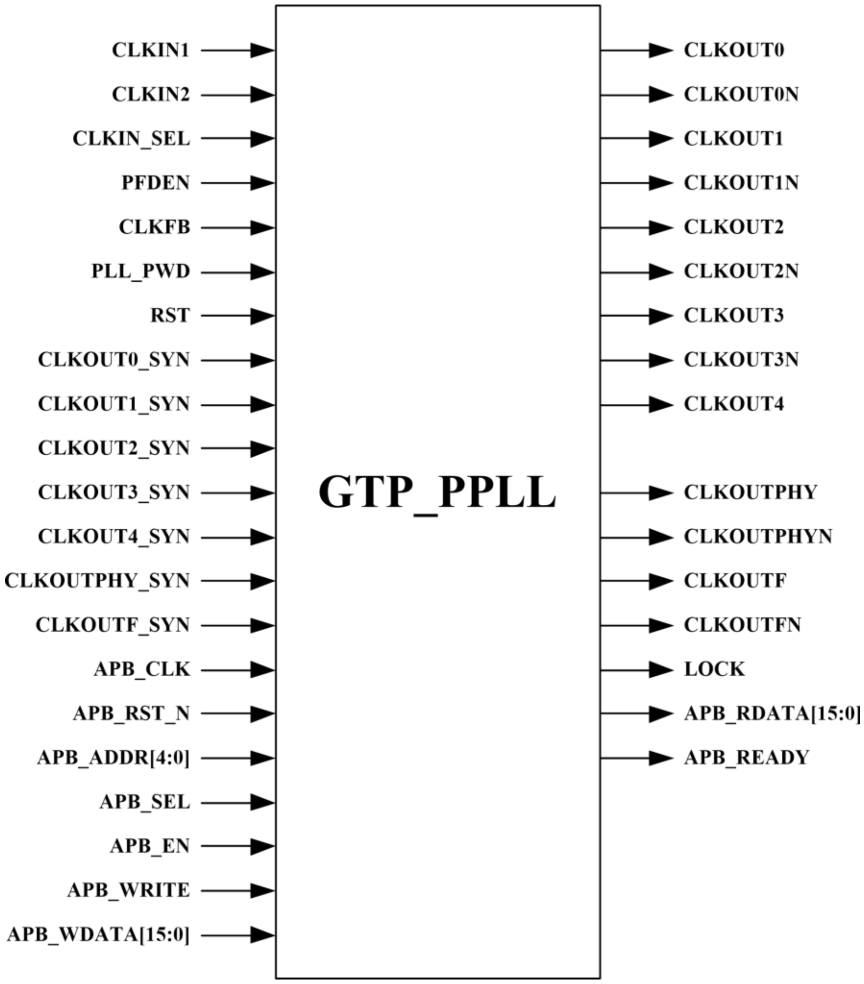


Figure 62 GTP_PPLL Block Diagram

3. GTP_PPLL port list

Table 34 GTP_PPLL port list

Port	I/O	Functional description
CLKOUT0	O	The positive phase output clock of the 0th channel of PLL;
CLKOUT0N	O	PLL channel 0 inverted output clock;
CLKOUT1	O	PLL No. 1 non-inverting output clock;
CLKOUT1N	O	PLL 1st channel inverted output clock;
CLKOUT2	O	PLL No. 2 non-inverting output clock;
CLKOUT2N	O	PLL No. 2 inverted output clock;
CLKOUT3	O	PLL No. 3 positive phase output clock;
CLKOUT3N	O	PLL No. 3 inverted output clock;
CLKOUT4	O	PLL No. 4 positive phase output clock;
CLKOUTPHY	O	PLL to DDR PHY positive phase output clock;
CLKOUTPHYN	O	PLL inverts output clock to DDR PHY;
CLKOUTF	O	PLL feedback positive phase output clock;
CLKOUTFN	O	PLL feedback inverting output clock;

Port	I/O	Functional description
LOCK	O	PLL frequency lock indication signal, which is an asynchronous signal; When the signal is pulled high, it indicates that the PLL feedback clock signal has been locked to the input clock signal;
APB_RDATA[15:0]	O	PLL APB interface data bus data output;
APB_READY	O	PLL APB interface data bus handshake signal; indicates the end of a normal bus cycle;
CLKIN1	I	PLL reference input clock 1;
CLKIN2	I	PLL reference input clock 2;
CLKFB	I	PLL feedback clock;
CLKIN_SEL	I	input clock selection signal;
PLL_PWD	I	PLL Power Down; active high;
RST	I	PLL reset signal, active high;
CLKOUT0_SYN	I	CLKOUT0/N output clock enable control; high level active; high level off, low level enable;
CLKOUT1_SYN	I	CLKOUT1/N output clock enable control; high level active; high level off, low level enable;
CLKOUT2_SYN	I	CLKOUT2/N output clock enable control; high level active; high level off, low level enable;
CLKOUT3_SYN	I	CLKOUT3/N output clock enable control; high level active; high level off, low level enable;
CLKOUT4_SYN	I	CLKOUT4 output clock enable control; high level active; high level off, low level enable;
CLKOUTPHY_SYN	I	CLKOUTPHY Output clock enable control; high level active; high level off, low level enable；
CLKOUTF_SYN	I	CLKOUTF/N output clock enable control; high level active; high level off, low level enable;
APB_CLK	I	PLL APB interface data bus clock;
APB_RST_N	I	PLL APB interface data bus asynchronous reset signal, active low;
APB_ADDR	I	PLL APB interface data bus address;
APB_SEL	I	PLL APB interface data bus selection signal, select slave device;
APB_EN	I	PLL APB interface data bus enable signal;
APB_WRITE	I	PLL APB interface data bus write enable signal; 1’b0: read operation, 1’b1: write operation;
APB_WDATA[15:0]	I	PLL APB interface data bus data input;

Note：

In the software process, the PPLL output is inserted into the USCM, and the global clock network is given priority. If you want to change the clock network, you can set it through the PAP_CLOCK_ASSIGN attribute. For detailed usage, refer to "User_Constraint_Editor_User_Guide".

3.1 Detailed description of GTP_PPLL interface

- CLKIN1

CLKIN1 is the main reference clock input, which can be directly driven by GMCLK and GSCLK in the same area, or GMCLK and GSCLK can drive all PPLLs on the same left side or right side through the PLL clock tree, can be driven by RCKB and HCKB in the same area, and can also be driven by SRB driver (not recommended), PPLL can be cascaded directly, and CLKOUT0~3/N can be used as CLKIN1 input to realize cascading.

- CLKIN2

CLKIN2 is a secondary input clock that is often used in applications that dynamically switch reference clocks. CLKIN2 can be directly driven by GMCLK and GSCLK in the same region, or GMCLK and GSCLK can drive all GPLLs on the same left or left side through the PLL clock tree, It can be driven by RCKB and HCKB in the same area, and can also be driven by SRB (not recommended). CLKOUT0~3/N can be cascaded as CLKIN2 input.

- CLKFB

CLKFB Feedback clock input, connected with external feedback output clock CLKOUTF as FPGA internal feedback, also can come in through clock input pin GMCLK/GSCLK and connect to CLKFB through GCLK_IBUF/USCM/HCKB as GPLL feedback clock, can be used for external clock alignment (reference clock and the feedback clock need to go through the same type of clock buffer).

- CLKOUTF

Feedback clock output, supports variable duty cycle, variable frequency (supports fractional frequency division), phase adjustment (only supported as an ordinary clock output port, phase cannot be adjusted when used as a feedback clock) and can be turned off or on, and can drive USCM /HCKB, see the GTP_PPLL application mode in Section 8 of this chapter for conventional applications.

- CLKOUTFN

The inverted output clock of CLKOUTF cannot be used as a feedback output clock.

- CLKIN_SEL

Select the input reference clock control signal, CLKIN_SEL=0, CLKIN1 is selected, CLKIN_SEL=1, CLKIN2 is selected, and the PPLL needs to be reset when the input clock is switched.

- PLL_PWD

Power-off control signal, when some modules do not need to work, PPLL can be turned off to reduce power consumption.

- APB configuration interface

The APB interface is a dynamic configuration interface, which can configure the output clock frequency, phase, duty cycle, etc. For details, please refer to the PPLL APB interface configuration in Section 5 of this chapter. When using the dynamic configuration function, you need to reset the PPLL and must operate according to the specified interface timing. , otherwise the configuration may be abnormal.

- CLKOUT0~4_SYN, CLKOUTF_SYN

Output clock enable signal, turn off the output clock at a high level, when the module driven by a certain clock output by PPLL does not need to work, the clock can be turned off, and the clock is not provided to the module to reduce power consumption.

- CLKOUT0~4

Output clock interface, each output clock is obtained by VCO frequency division (see Figure 61 for details), default phase alignment, each channel supports phase shift, variable duty cycle, variable frequency and can be turned off or on , only CLKOUT0 supports fractional frequency division.

When the PPLL output clock is to drive RCKB or IOCKB, only CLKOUT0~3 can be selected, and these 4 outputs can all drive USCM and HCKB; CLKOUT0~3 outputs can also be used as other GPLL/PPLL inputs with the PLL clock tree to achieve level link function.

- CLKOUT0~3N

CLKOUT0~3N is the 180° reverse clock output of CLKOUT0~3.

- LOCK

The LOCK signal is used to indicate when the phase alignment of the input reference clock (CLKIN1/CLKIN2) and the feedback input clock has been locked to the input clock signal.

4. GTP_PPLL parameter list

Table 35 GTP_PPLL parameter list

Parameter name	Parameter Type	Valid value	Defaults	Functional description
CLKIN_FREQ	real	19~800	50.0	Input clock frequency configuration, MHz;
LOCK_MODE	binary	1’b0,1’b1	1’b0	PLL frequency detection mode configuration; 1’b0: Real-time monitoring of PLL working status; 1’b1: LOCK 1 is kept after PLL is locked, unless reset or Power Down;
STATIC_RATIOI	interger	1-40	1	Enter the divider ratio static configuration;
STATIC_RATIOM	interger	1-128	1	Feedback M divider ratio static configuration;
STATIC_RATIO0	interger	1-128	1	output divider0 ratio static configuration;
STATIC_RATIO1	interger	1-128	1	output divider1 ratio static configuration;
STATIC_RATIO2	interger	1-128	1	output divider2 ratio static configuration;
STATIC_RATIO3	interger	1-128	1	output divider3 ratio static configuration;
STATIC_RATIO4	interger	1-128	1	output divider4 ratio static configuration;
STATIC_RATIOPHY	interger	1-128	1	Output dividerphy ratio static configuration;
STATIC_RATIOF	interger	1-128	1	Feedback F divider ratio static configuration;
STATIC_DUTY0	interger	2~255	2	output divider0 duty static configuration;
STATIC_DUTY1	interger	2~255	2	output divider1 duty static configuration;
STATIC_DUTY2	interger	2~255	2	output divider2 duty static configuration;
STATIC_DUTY3	interger	2~255	2	output divider3 duty static configuration;
STATIC_DUTY4	interger	2~255	2	output divider4 duty static configuration;
STATIC_DUTYPHY	interger	2~255	2	Output dividerphy duty static configuration;
STATIC_DUTYF	interger	2~255	2	Feedback F divider duty static configuration;
STATIC_PHASE0	interger	0-7	0	output divider0 fine phase static configuration;
STATIC_PHASE1	interger	0-7	0	output divider1 fine phase static configuration;
STATIC_PHASE2	interger	0-7	0	output divider2 fine phase static configuration;
STATIC_PHASE3	interger	0-7	0	output divider3 fine phase static configuration;
STATIC_PHASE4	interger	0-7	0	output divider4 fine phase static configuration;
STATIC_PHASEPHY	interger	0-7	0	Output dividerphy fine phase static configuration;
STATIC_PHASEF	interger	0-7	0	Feedback F divider fine phase static configuration;
STATIC_CPHASE0	interger	0-127	0	output divider0 coarse phase static configuration;
STATIC_CPHASE1	interger	0-127	0	output divider1 coarse phase static configuration;
STATIC_CPHASE2	interger	0-127	0	output divider2 coarse phase static configuration;
STATIC_CPHASE3	interger	0-127	0	output divider3 coarse phase static configuration;
STATIC_CPHASE4	interger	0-127	0	output divider4 coarse phase static configuration;
STATIC_CPHASEPHY	interger	0-127	0	Output dividerphy coarse phase static configuration;
STATIC_CPHASEF	interger	0-127	0	Feedback F divider coarse phase static configuration;
CLKOUT0_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUT0_SYN signal enable configuration;
CLKOUT1_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUT1_SYN signal enable configuration;
CLKOUT2_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUT2_SYN signal enable configuration;
CLKOUT3_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUT3_SYN signal enable configuration;
CLKOUT4_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUT4_SYN signal enable configuration;

Parameter name	Parameter Type	Valid value	Defaults	Functional description
CLKOUTPHY_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUTPHY_SYN signal enable configuration;
CLKOUTF_SYN_EN	string	"FALSE", "TRUE"	"FALSE"	CLKOUTF_SYN signal enable configuration;
INTERNAL_FB	string	"CLKOUT0", "CLKOUT1", "CLKOUT2", "CLKOUT3", "CLKOUT4", "CLKOUTF", "DISABLE"	"CLKOUTF"	Internal feedback path selection, select one of these output clocks as the internal feedback clock, such as INTERNAL_FB = " CLKOUT0", then the output clock CLKOUT0 is used as the internal feedback clock;
EXTERNAL_FB	string	"CLKOUT0", "CLKOUT1", "CLKOUT2", "CLKOUT3", "CLKOUT4", "CLKOUTF", "DISABLE"	"DISABLE"	External feedback path selection, select one of these output clocks as the external feedback clock, such as EXTERNAL_FB = " CLKOUT0", then output Clock CLKOUT0 as internal feedback clock;
BANDWIDTH	string	"LOW", "HIGH" "OPTIMIZED"	"OPTIMIZED"	Bandwidth selection configuration: BANDWIDTH="LOW" is configured as "LOW", BANDWIDTH="HIGH" is configured as "HIGH" BANDWIDTH="OPTIMIZED" is configured as "OPTIMIZED";

Note:

(1) The parameters INTERNAL_FB and EXTERNAL_FB cannot be configured as "DISABLE" at the same time;

(2) PFD configured with "LOW", "OPTIMIZED" and "HIGH" of BANDWIDTH is limited by PFD frequency, see Table 38 for details;

5. GTP_PPLL APB interface configuration

5.1 Configure interface

The user logic dynamically changes the GTP_PPLL working parameters through the APB interface. The sequence of reading and writing registers of the APB interface is shown in Figure 63~Figure 66.

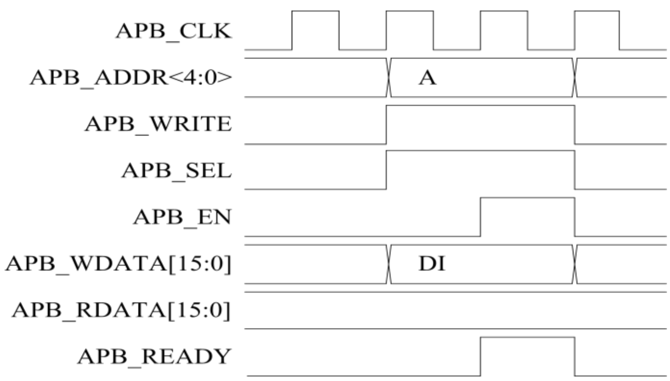


Figure 63 GTP_PPLL_APB Write Timing

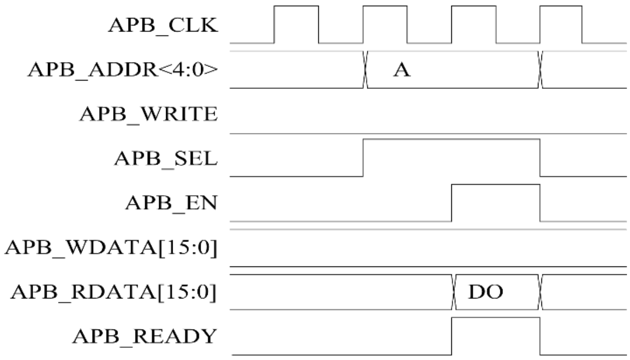


Figure 64 GTP_PPLL_APB Read Timing

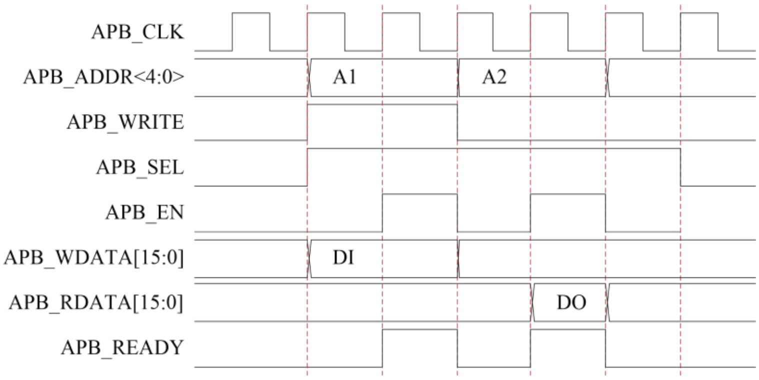


Figure 65 GTP_PPLL_APB Read After Write Timing

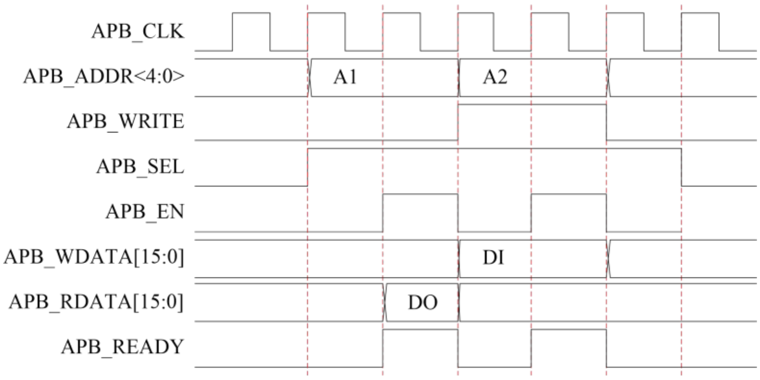


Figure 66 GTP_PPLL_APB interface read-after-write timing

Table 36 GTP_PPLL_APB interface port list

Serial number	Port name	I/O	Description
1	APB_CLK	I	Clock, rising edge sampling;
2	APB_RST_N	I	Asynchronous reset, active low; only reset Data Bus (do not reset registers);
3	APB_ADDR[4:0]	I	Address bus;
4	APB_SEL	I	Select, indicating that the slave device is selected;
5	APB_EN	I	Enable, bus enable signal;
6	APB_WRITE	I	Direction, 0: read, 1: write;
7	APB_WDATA[15:0]	I	Data bus input;
8	APB_RDATA[15:0]	O	Data bus output;
9	APB_READY	O	Sign signal;

System application requirements for writing internal registers via APB interface:

(1) After the APB rewrites the internal registers, it is necessary to reset the PLL to ensure its normal operation;

(2) The minimum pulse width of TRST is 10ns;

5.2 Configuration registers

Table 37 GTP_PPLL_APB interface register list

Address	Bit	Register	Description
0	[15:8]	REG_ODIV0_RATIO<7:0>,	ODIV0 Register1: frequency division ratio setting;
	[7:0]	REG_ODIV0_DUTY<7:0>	ODIV0 Register1: duty cycle setting;
1	[15:11]	RESERVED	
	[10]	REG_ODIV0_MUXSEL_EN	ODIV0 Register2: input clock MUX enable;
	[9:7]	REG_ODIV0_FPHASE<2:0>	ODIV0 Register2: phase fine adjustment setting;
	[6:0]	REG_ODIV0_CPHASE<6:0>	ODIV0 Register2: coarse phase adjustment setting;
2	[15:8]	REG_ODIV1_RATIO<7:0>	ODIV1 Register1: frequency division ratio setting;
	[7:0]	REG_ODIV1_DUTY<7:0>	ODIV1 Register1: duty ratio setting;
3	[15:11]	RESERVED	
	[10]	REG_ODIV1_MUXSEL_EN	ODIV1 Register2: input clock MUX enable;
	[9:7]	REG_ODIV1_FPHASE<2:0>	ODIV1 Register2: phase fine adjustment setting;
	[6:0]	REG_ODIV1_CPHASE<6:0>	ODIV1 Register2: coarse phase adjustment setting;
4	[15:8]	REG_ODIV2_RATIO<7:0>	ODIV2 Register1: frequency division ratio setting;
	[7:0]	REG_ODIV2_DUTY<7:0>	ODIV2 Register1: duty cycle setting;
5	[15:11]	RESERVED	
	[10]	REG_ODIV2_MUXSEL_EN	ODIV2 Register2: input clock MUX enable;
	[9:7]	REG_ODIV2_FPHASE<2:0>	ODIV2 Register2: phase fine adjustment setting;
	[6:0]	REG_ODIV2_CPHASE<6:0>	ODIV2 Register2: coarse phase adjustment setting;
6	[15:8]	REG_ODIV3_RATIO<7:0>	ODIV3 Register1: frequency division ratio setting;
	[7:0]	REG_ODIV3_DUTY<7:0>	ODIV3 Register1: duty ratio setting;
7	[15:11]	RESERVED	
	[10]	REG_ODIV3_MUXSEL_EN	ODIV3 Register2: input clock MUX enable;
	[9:7]	REG_ODIV3_FPHASE<2:0>	ODIV3 Register2: phase fine adjustment setting;
	[6:0]	REG_ODIV3_CPHASE<6:0>	ODIV3 Register2: coarse phase adjustment setting;
8	[15:8]	REG_ODIV4_RATIO<7:0>	ODIV4 Register1: frequency division ratio setting;
	[7:0]	REG_ODIV4_DUTY<7:0>	ODIV4 Register1: duty ratio setting;
9	[15:11]	RESERVED	
	[10]	REG_ODIV4_MUXSEL_EN	ODIV4 Register2: input clock MUX enable;
	[9:7]	REG_ODIV4_FPHASE<2:0>	ODIV4 Register2: phase fine adjustment setting;
	[6:0]	REG_ODIV4_CPHASE<6:0>	ODIV4 Register2: coarse phase adjustment setting;
A	[15:8]	REG_ODIVPHY_RATIO<7:0>	ODIVPHY Register1: frequency division ratio setting;
	[7:0]	REG_ODIVPHY_DUTY<7:0>	ODIVPHY Register1: duty cycle setting;
B	[15:11]	RESERVED	
	[10]	REG_ODIVPHY_MUXSEL_EN	ODIVPHY Register2: input clock MUX enable;
	[9:7]	REG_ODIVPHY_FPHASE<2:0>	ODIVPHY Register2: phase fine adjustment setting;
	[6:0]	REG_ODIVPHY_CPHASE<6:0>	ODIVPHY Register2: coarse phase adjustment setting;
C	[15:8]	REG_FDIV_RATIO<7:0>	FDIV Register1: frequency division ratio setting;
	[7:0]	REG_FDIV_DUTY<7:0>	FDIV Register1: duty cycle setting;
D	[15:11]	RESERVED	
	[10]	REG_FDIV_MUXSEL_EN	FDIV Register2: input clock MUX enable;
	[9:7]	REG_FDIV_FPHASE<2:0>	FDIV Register2: phase fine adjustment setting;
	[6:0]	REG_FDIV_CPHASE<6:0>	FDIV Register2: coarse phase adjustment setting;

Address	Bit	Register	Description
E	[15:7]	RESERVED	
	[6:0]	REG_IDIV_RATIO<7:0>	IDIV Register: frequency division ratio setting;
F	[15:7]	RESERVED	
	[6:0]	REG_MDIV_RATIO<7:0>	MDIV Register: frequency division ratio setting;
10	[15:14]	RESERVED	BANDWIDTH Register
	[13:12]	REG_VCTRL_INIT<1:0>	
	[11:10]	REG_CP_SELFBIAS_SEL<1:0>	
	[9:8]	REG_ICP_BASE_SEL<1:0>	
	[7:4]	REG_CP_CUR_SEL<3:0>	
	[3:1]	REG_LPF_R<2:0>	
	[0]	REG_LPF_C	
11	[15:6]	RESERVED	LOCK Register1
	[5]	REG_LOCK_FILTER_PD	
	[4:0]	REG_FREQ_LOCKDET_SET<4:0>	

Detailed function description:

1. BANDWIDTH Register

BANDWIDTH Register is the loop bandwidth register, the specific parameters are as follows:

Table 38 PPLL BANDWIDTH Register parameter list

BANDWIDTH	PFD reference frequency range	Feedback divider	REG_CP_ SELFBIAS_SEL	REG_ICP_ BASE_SEL	REG_CP_ CUR_SEL	REG_ LPF_R	REG_ LPF_C
LOW OPTIMIZED	19<=F<=80MHz	12~15	1	1	3	4	0
		16~19			4		
		20~23			5		
		24~27			6		
		28~31			7		
		32~35			12		
		36~39			13		
		40~43			14		
		44~47			15		
		48~54		2	6		
		55~59			7		
		60~69		3	5		
		70~79		2	12		
		80~89			14		
		90~99			15		

BANDWIDTH	PFD reference frequency range	Feedback divider	REG_CP_ SELFBIAS_SEL	REG_ICP_ BASE_SEL	REG_CP_ CUR_SEL	REG_ LPF_R	REG_ LPF_C
		100~106		3	12		
		107~112			13		
HIGH	80<=F<=450MHz	2	1	2	2	0	0
		3			3		
		4			4		
		5			5		
		6			6		
		7			7		
		8			12		
		9			13		
		10			14		
		11			15		
		12~13		3	12		
		14~15			13		
		16~19			14		
		20~23			13	1	
		24~28			14		
Remark			1: PFD reference frequency: CLKIN_FREQ/STATIC_RATIOI; 2: INTERNAL_FB is "CLKOUT0~4/F"; EXTERNAL_FB is "DISABLE"; Feedback divider = STATIC_RATIO0~4/F*STATIC_RATIOM; INTERNAL_FB is "DISABLE"; EXTERNAL_FB is "CLKOUT0~4/F"; Feedback divider = STATIC_RATIO0~4/F*STATIC_RATIOM;				

2. Other registers

For other register configuration methods, refer to Section 5.2 of Chapter 2 GPLL Instructions. PPLL does not support fractional frequency division, only integer frequency division.

5.3 Configuration restrictions

During dynamic configuration, there will be some restrictions. For the configuration parameter range, refer to Table 35. The input clock frequency range, VCO frequency range, and output frequency range are shown in the following table:

Table 39 Operating frequency range

Parameter	Description	Minimum value	Typical value	Maximum Value	Unit
F_{IN}	Input clock frequency	19		800	MHz
F_{VCO}	VCO operating frequency range	1330		2133	MHz
F_{OUT}	Output Clock Frequency Range	10.39		2133	MHz

Note: Please refer to Section 6.5 of this chapter for the calculation of F_{VCO} and F_{OUT};

6. GTP_PPLL function description

6.1 Clock input

When CLKIN_SEL is 0, select CLKIN1; when CLKIN_SEL is 1, select CLKIN2. The reference clock is dynamically switched between CLKIN1 and CLKIN2, and the PLL needs to be reset after switching.

For the PPLL input clock, the following points should be noted:

- When the input clock is lost or unstable, the LOCK signal of the PPLL is pulled low, and the PPLL must be reset after recovery again.
- If there is no reference clock after power-on and power-on, the PPLL will output a low-frequency clock signal. At this time, the LOCK signal is low. If you want the output clock to be 0, you can use power-off mode or clock output gating. For details, see Sections 6.3 and 6.10.

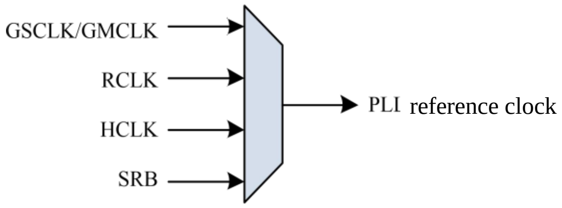


Figure 67 GTP_PPLL Reference Clock Source

6.2 PPLL reset

After the RST reset signal is released, the PLL starts to enter the lock state, and the PLL frequency lock is completed after the TLOCK time. The timing of the RST reset signal is shown in the figure below, and the high level is valid.

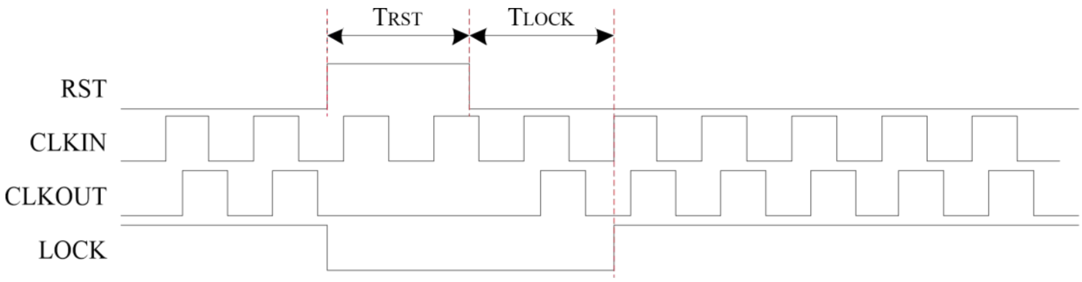


Figure 68 GTP_PPLL Reset Timing

The minimum pulse width of T_{RST} is 10ns, and the maximum lock time of T_{LOCK} is 120us.

6.3 PPLL Power Off

When PLL is not used, PLL_PWD=1, PLL can be turned off to save power.

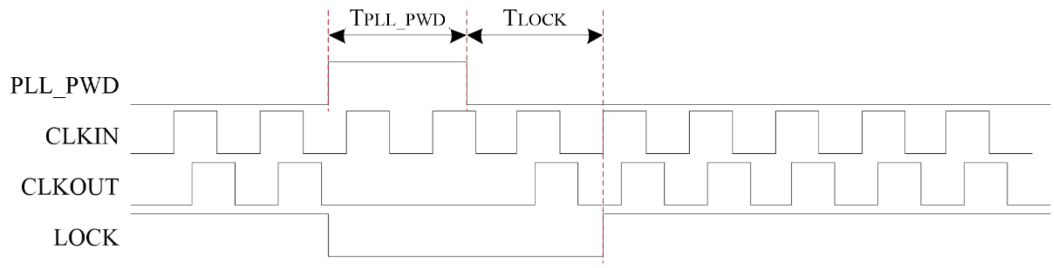


Figure 69 GTP_PPLL power-off sequence

The minimum pulse width of T_{PLL_PWD} is 5ns, and the maximum lock time of T_{LOCK} is 120us.

6.4 Feedback clock selection

The feedback clock input source of PPLL can be divided into PPLL internal feedback and PPLL external feedback, and the feedback source supports CLKOUT[0]~CLKOUT[4], CLKOUTF. By default, the internal feedback clock selects CLKOUTF.

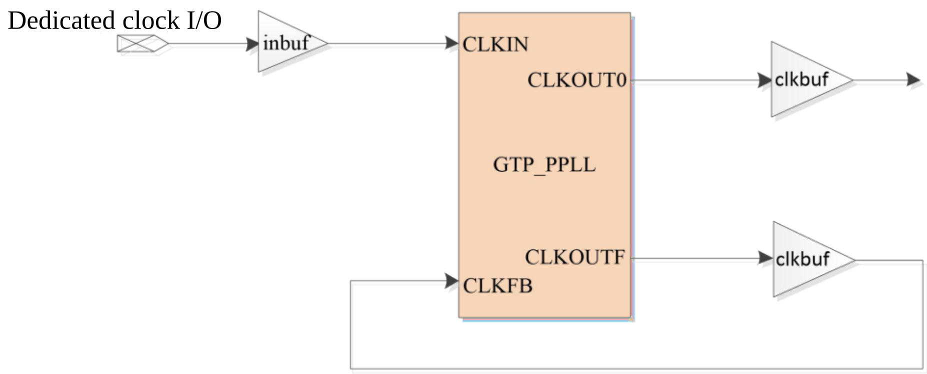


Figure 70 GTP_PPLL External Feedback Diagram

As shown in the figure, when external feedback is selected, the feedback clock reaches the feedback clock input through a dedicated clock path through the global clock or horizontal clock buffer. In internal feedback mode, the feedback clock output directly reaches the feedback clock input inside the PLL. Minimal distraction.

Table 40 Feedback Clock Selection List

INTERNAL_FB	EXTERNAL_FB	Feedback mode
"CLKOUT0"	"DISABLE"	Internal feedback mode, select output divider0;
"CLKOUT1"	"DISABLE"	Internal feedback mode, select output divider1;
"CLKOUT2"	"DISABLE"	Internal feedback mode, select output divider2;
"CLKOUT3"	"DISABLE"	Internal feedback mode, select output divider3;
"CLKOUT4"	"DISABLE"	Internal feedback mode, select output divider4;
"CLKOUTF"	"DISABLE"	Internal feedback mode, select feedback F divider;
"DISABLE"	"CLKOUT0"	External feedback mode, select output divider0;
"DISABLE"	"CLKOUT1"	External feedback mode, select output divider1;
"DISABLE"	"CLKOUT2"	External feedback mode, select output divider2;
"DISABLE"	"CLKOUT3"	External feedback mode, select output divider3;
"DISABLE"	"CLKOUT4"	External feedback mode, select output divider4;
"DISABLE"	"CLKOUTF"	External feedback mode, select feedback F divider;

6.5 Output frequency programming

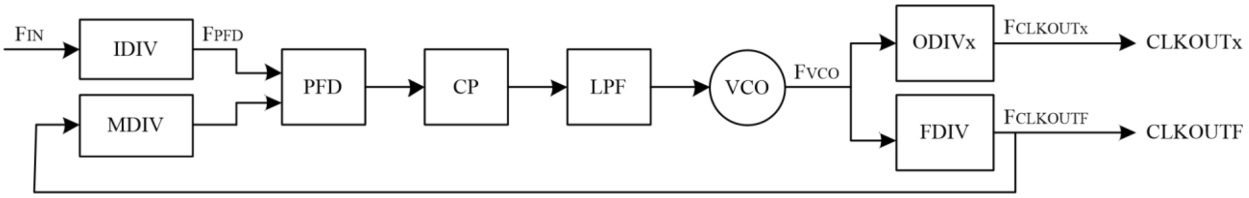


Figure 71 GTP_PPLL output frequency programming diagram

The reference clock (Fin) passes through the programmable input frequency divider (IDIV) to obtain a reference clock of the phase frequency detector (PFD), and the feedback clock passes through the programmable feedback frequency divider (FDIV) and (MDIV) to obtain the other 1 of the PFD A reference clock, PFD compares the phase and frequency of these two clocks, and then generates a signal to drive the charge pump (CP), the current signal generated by CP passes through the loop filter (LPF), and the LPF generates a reference voltage for the voltage control Oscillator (VCO); PFD provides CP and LPF with phase leading or lagging signals to continuously adjust the frequency of VCO operation to adjust frequency and phase. For example, when VCO is still higher than the reference frequency after passing through the feedback frequency divider, PFD generates A downward adjustment signal makes CP and LPF reduce the voltage to control VCO to reduce the output frequency. When VCO is still lower than the reference frequency after passing through the feedback frequency divider, PFD generates an upward adjustment signal to make CP and LPF increase the voltage Control the VCO to increase the output frequency. The VCO generates 8-phase output clocks, which can realize phase shift coarse adjustment and fine adjustment through the 8-phase clocks. Each output phase shift clock can be used as the input of FDIV. There are 7 output frequency dividers in total, 6 ODIV and 1 FDIV, each frequency divider is independent, and the clock output by the VCO passes through these frequency dividers to obtain the final output clock frequency.

Table 41 PPLL output frequency programming parameter description

No.	GTP parameters	Function name	Description
1	CLKIN_FREQ	FIN	Reference clock frequency;
2	STATIC_RATIOI	FPFD	The PFD input reference frequency is determined by the GTP parameter configuration frequency division coefficient in the list;
3	STATIC_RATIOF , STATIC_RATIOI, STATIC_RATIOM	FVCO	The VCO output clock frequency is determined by the GTP parameter configuration frequency division coefficient in the list;
4	STATIC_RATIOF, STATIC_RATIOI, STATIC_RATIOM, STATIC_RATIO0~4,STATIC_RATIOPHY	FCLKOUTx	CLKOUTx output clock frequency is determined by the GTP parameter configuration frequency division coefficient in the list, x represents 0~4/PHY, STATIC_RATIO0~4 corresponds to CLKOUT0~4, STATIC_RATIOPHY corresponds to CLKOUTPHY;
5	STATIC_RATIOF	FCLKOUTF	CLKOUTF output clock frequency is determined by the GTP parameter configuration frequency division coefficient in the list;
6	STATIC_RATIOI	IDIV	Input frequency divider frequency division ratio;
7	STATIC_RATIOM	MDIV	Feedback Divider M Division Ratio
8	STATIC_RATIO0~4, STATIC_RATIOPHY	ODIVx	Output divider frequency division ratio, x represents 0~4/PHY, STATIC_RATIO0~4 corresponds to CLKOUT0~4, STATIC_RATIOPHY corresponds to CLKOUTPHY;
9	STATIC_RATIOF	FDIV	Feedback divider F division ratio;

Note: CLKIN_FREQ is the default configuration parameter of the input clock frequency, not the input interface of the PLL. The input interface refers to CLKIN1 and CLKIN2 in Figure 62; the input and output frequency, PFD frequency range, etc. refer to the data sheet "DS05001".

If the frequency division ratio of the feedback frequency divider selected by internal feedback or external feedback is FBDIV, the calculation formula of each clock frequency is as follows:

$$F_{PFD} = \frac{F_{IN}}{IDIV}$$

$$F_{VCO} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV}$$

$$F_{CLKOUTx} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV \times ODIVx}$$

$$F_{CLKFBOUT} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV \times FDIV}$$

Among them, FBDIV is the frequency division ratio of the frequency divider selected by the feedback loop, FBDIV∈[ODIV0~4,FDIV], for example, when the feedback clock is CLKOUT0, FBDIV=ODIV0.

6.6 Loop Bandwidth

PPLL loop bandwidth can be configured as low bandwidth (LOW), medium bandwidth (OPTIMIZED) and high bandwidth (HIGH). The parameters of low bandwidth and medium bandwidth configuration are the same, see Table 38 for details.

Considering that the input clock is not an ideal clock in practical applications, different bandwidth configurations have different effects on the PLL:

(1) If the PLL output clock is expected to have a small Jitter, configure it as low bandwidth or medium bandwidth, and the locking time is long at this time;

(2) If the PLL lock time is expected to be short, configure it as high bandwidth, and the output clock Jitter will become worse at this time;

6.7 Phase adjustment

Phase adjustment includes phase coarse adjustment and phase fine adjustment. The phase coarse adjustment and phase fine adjustment can be adjusted through static configuration or through the APB interface. These two adjustment methods are independent of each other. Each clock output is used as a feedback clock The output clock cannot be phase adjusted.

(1) Phase adjustment method:

➢ Phase coarse adjustment

The coarse phase adjustment of the output clock CLKOUT0/1/2/3/4/F and CLKOUTPHY can be realized by configuring the parameters STATIC_CPHASE0/1/2/3/4/F and STATIC_CPHASEPHY. Refer to Table 35 for the parameter configurable range.

Relative to the input VCO clock, the coarse adjustment time step of the output clock phase is Tvco, the adjustment range is [0~Ndiv-1]*Tvco, and the adjustment degree step is 360°/Ndiv.

Ndiv is the output divider ODIVx and the feedback divider FDIV.

For example, the frequency division factor Ndiv of the output clock CLKOUT0 is 6. According to the formula, the degree of each adjustment is 60°, and the parameter configuration takes an integer multiple of Ndiv as one cycle, then the corresponding relationship between the configurable phase of CLKOUT0 and STATIC_CPHASE0 is as follows:

STATIC_CPHASE0=0, CLKOUT0 phase shift 0°;

STATIC_CPHASE0=1, CLKOUT0 phase shift 60°;

STATIC_CPHASE0=2, CLKOUT0 phase shift 120°;

STATIC_CPHASE0=3, CLKOUT0 phase shift 180°;

STATIC_CPHASE0=4, CLKOUT0 phase shift 240°;

STATIC_CPHASE0=5, CLKOUT0 phase shift 300°;

STATIC_CPHASE0=6, CLKOUT0 phase shift 0°.

➢ Phase fine adjustment

By configuring the parameters STATIC_PHASE0/1/2/3/4/F and STATIC_PHASEPHY, the phase fine adjustment of the output clock CLKOUT0/1/2/3/4/F and CLKOUTPHY can be realized, and the parameter configurable range can be referred to Table 35.

Relative to the input VCO clock, the fine adjustment time step of the output clock phase is Tvco, the adjustment range is (0~7/8)Tvco, the adjustment degree step is 45°/Ndiv, and the adjustment range is (0°~45° *7)/Ndiv.

For example, the VCO frequency is 1000MHz, and the output frequency division factor of CLKOUT0 is 24. According to the formula, the time for each adjustment is 125ps, the adjustment range is 0ps~875ps, the degree of single adjustment is 1.875°, and the adjustment range is 0°~13.125°.

STATIC_CPHASE0=0, the corresponding relationship between CLKOUT0 configurable phase and STATIC_PHASE0 is as follows:

STATIC_PHASE0=0, CLKOUT0 phase shift 0°

STATIC_PHASE0=1, CLKOUT0 phase shift 1.875°;

STATIC_PHASE0=2, CLKOUT0 phase shift 3.750°;

STATIC_PHASE0=3, CLKOUT0 phase shift 5.625°;

STATIC_PHASE0=4, CLKOUT0 phase shift 7.50 0°;

STATIC_PHASE0 =5, CLKOUT0 phase shift is 9.375°;

STATIC_PHASE0=6, CLKOUT0 phase shift is 11.250°;

STATIC_PHASE0=7, CLKOUT0 phase shift is 13.125°.

Note:

- Ndiv∈{STATIC_RATIO0~6, STATIC_RATIOF}, is the frequency division coefficient of the output clock CLKOUT0/1/2/3/4/5/6/F, the parameters can be configured refer to the GTP_GPLL parameter list, Tstep each phase adjustment time variable , Dstep is the degree variable for each phase adjustment.

(2) Phase adjustment mode:

- Static configuration
- The output clock CLKOUT0/1/2/3/4/PHY/F phase fine-tuning static configuration is controlled by STATIC_PHASE0/1/2/3/4/PHY/F respectively;
- The output clock CLKOUT0/1/2/3/4/PHY/F phase coarse adjustment static configuration is controlled by STATIC_CPHASE0/1/2/3/4/PHY/F respectively;

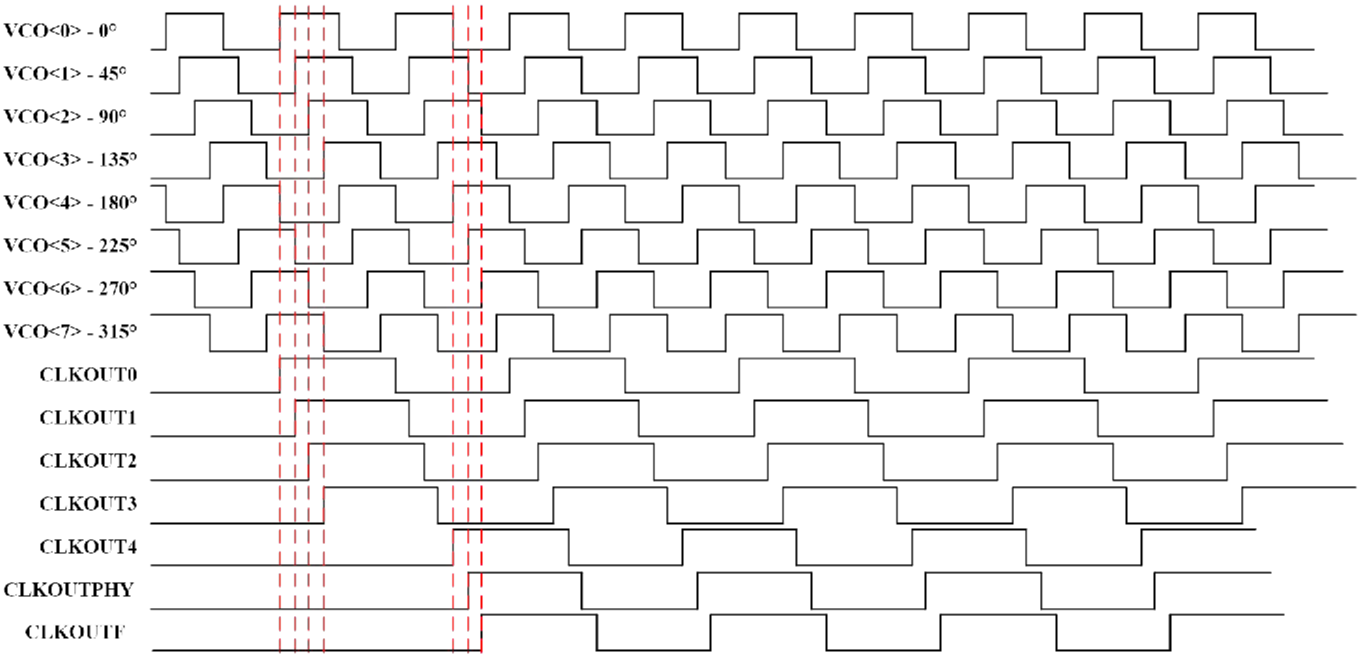


Figure 72 GTP_PPLL phase adjustment_static configuration

As shown in the table below, CLKOUT0 is generated by frequency division of VCO<0>2, the phase of fine adjustment is 0, and the phase of coarse adjustment is 0. Taking CLKOUT0 as the reference, the phase relationship of each output clock is as follows:

Note: According to the formula, since ODIV0=2, the minimum fine phase step=45°/2=22.5°, and the minimum coarse phase step=180°

Table 42 Output Clock Phase Relationship

Output clock	Fine tune configuration	Coarse configuration	Phase relationship
CLKOUT0	0	0	0
CLKOUT1	1*Tvco/8	0	22.5°
CLKOUT2	2*Tvco/8	0	45°
CLKOUT3	3*Tvco/8	0	67.5°
CLKOUT4	4*Tvco/8	Tvco	270°
CLKOUTPHY	5*Tvco/8	Tvco	292.5°
CLKOUTF	6*Tvco/8	Tvco	315°

6.8 Programmable Duty Cycle

The output divider supports programmable Duty Cycle. The minimum step is 50%/odiv, and odiv is the frequency division coefficient of the divider. STATIC_DUTY0/1/2/3/4/PHY/F determines the duty cycle after frequency division. The expression is as follows, duty is duty cycle configuration value.

$$\text{duty cycle} = (50\%/\text{odiv})*\text{duty}$$

For example, if odiv is 24, then according to the formula, the duty range can be 2~47, and the duty cycle range is 4.17%~97.92%.

Note: (1) The setting value of DUTY is limited by the odiv value (output frequency division):

odiv >1,2=< duty <= 2* odiv -1;

odiv =1, duty is invalid, does not work, the default is 50% output.

(2) Fractional frequency division does not support duty cycle programming.

6.9 Spread Spectrum Clock Input

Support spectrum spread clock input, the modulation frequency is less than PPLL bandwidth;

6.10 Clock output gating

The GTP_PPLL input signal CLKOUT0_SYN is used to enable and disable the CLKOUT0 output clock. When the user does not need the CLKOUT0 clock, the clock can be turned off to save Clock Tree and Fabric power consumption.

CLKOUT0_SYN signal is optional, when the user configures CLKOUT0_SYN_EN as "TRUE", the signal is valid.

Similarly, the input signal CLKOUT1~4/PHY/F_SYN cooperates with the configuration bit CLKOUT1~4/PHY/F_SYN_EN to enable and disable the CLKOUT1~4/PHY/F clock.

Taking the output clock CLKOUT0 as an example, the functional diagram is shown in the figure below:

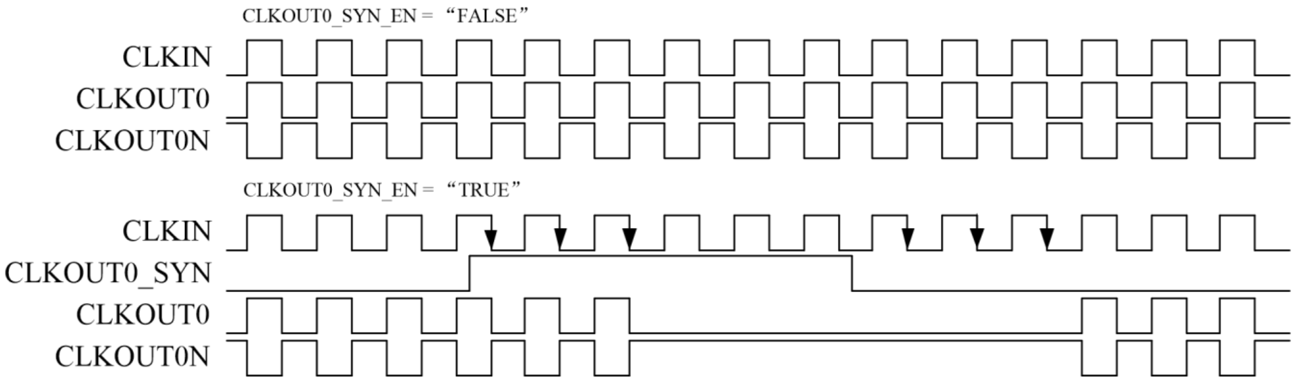


Figure 73 GTP_PPLL output clock GATE timing diagram

6.11 LOCK indication

PPLL supports two LOCK modes, which are selected by the configuration parameter LOCK_MODE.

Table 43 PPLL LOCK indication modes

Parameter name	Parameter value	Functional description
LOCK_MODE	0	Monitor the state of PLL LOCK in real time, once it enters an abnormal state, it will pull down LOCK.
	1	LOCK will not monitor (indicate) the PLL working status in real time; once LOCK 1 is pulled high, it will not be pulled low unless it is reset or Power Down.

7. GTP_PPLL configuration constraints

Refer to Section 7 of GTP_GPLL Configuration Constraints in Chapter 2 GPLL Instructions. The factors considered in the configuration parameters are the same as the related formulas, but it should be noted that some parameters can be configured in different ranges. The parameter range, input For output clock, VCO frequency range, etc., see Table 35 and Table 39.

8. GTP_PPLL application mode

8.1 Internal feedback mode

The internal feedback mode is mainly for certain application scenarios, which have high performance requirements for the PPLL output clock, such as frequency synthesis, low jitter clock output, etc.

In the internal feedback mode, the feedback clock is directly connected to the input of the PPLL without passing through any other circuits, which avoids the noise introduced by other circuits and has better jitter performance.

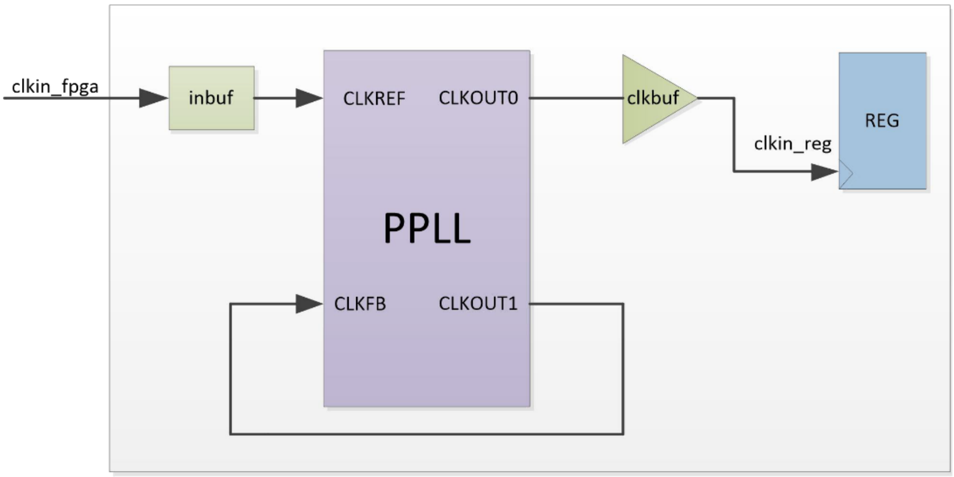


Figure 74 Schematic Diagram of PPLL Internal Feedback Mode

8.2 Source synchronous mode

Use external feedback to realize the source synchronous mode. The source synchronous mode is mainly for the PPLL output clock to drive the internal register. It is necessary to ensure that the input clock and the data maintain a certain phase relationship, as shown in the figure below. When the PPLL is locked, the phase of the b/e point is Aligned, in source synchronous mode, the path of the PPLL output clock clkout0 to the register and the path experienced by the feedback clock clkout1 must be symmetrically balanced, and use the same regional buffer, that is, to ensure that the clock phases of points c and e are aligned, that is Point b is aligned with the clock phase of point c; at the same time, the skew (offset) between the data pin to the register data terminal input and the clock pin to the PPLL input reference clock can be compensated through the PPLL phase adjustment function, that is, point d to point f And the offset from point a to point b, so that at the internal REG of FPGA, the phase edge or center alignment between data and clock can be realized, specifically 0° or 90° alignment, depending on the user's requirements, the specific phase shift The requirement can be realized by the phase shift function of the frequency divider of the output clock.

For example, if the rising edge of the input pin clock enters the FPGA at the center of the data, the PPLL output phase shift function can be used to move the phase of clkout0, and the registers inside the FPGA can align the rising edge of the clock to the center of the data. At this time, if there is no skew between the reference input of the input clock clkin_fpga entering the PPLL and the data entering the register, such as taking a dedicated clock path, that is, the skew is very small. At this time, the PPLL can automatically realize the above clock without any phase shift adjustment The rising edge is aligned with the center of the data center.

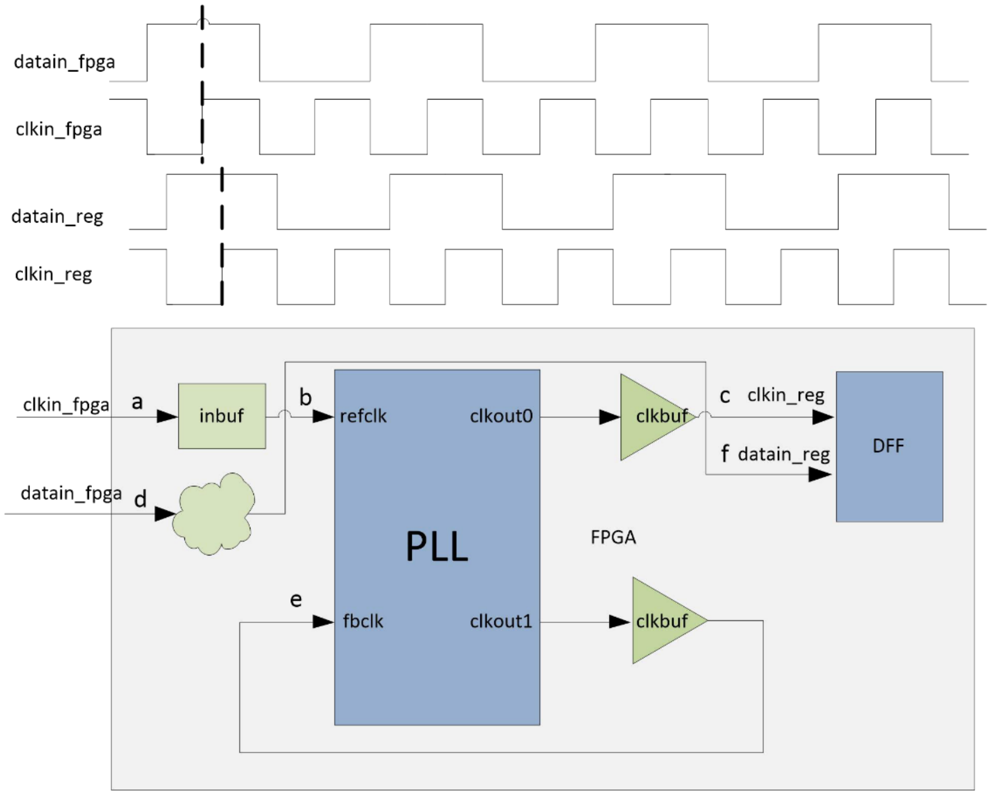


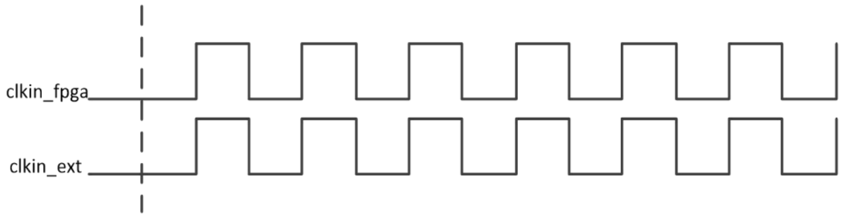
Figure 75 Schematic diagram of PPLL source synchronous mode

8.3 Zero Latency Mode

Using external pin feedback to achieve zero-delay mode is mainly for the case where there is only one input reference clock and the FPGA drives multiple external devices. It is necessary to ensure that the input clock of the external device is aligned with the clock of the FPGA input pin, as shown in the figure below Show.

In zero-delay mode, the input clock and the feedback clock need to use the same IO standard to ensure that point a is aligned with point d, and point b is aligned with point e. At the same time, the feedback clock trace on the board and the clock trace driving the external device If they match each other and are equal in length, the phases of the clocks at points d and c are aligned, so the clocks at points a and c are aligned to realize the function of zero-delay buffering.

In actual situations, due to the inconsistency between the load parasitic capacitance of the external device and the parasitic capacitance of the FPGA input pin, the timing of the rising or falling edge of the signal at point c and point d will be inconsistent, resulting in a slight difference in delay. Therefore The difference in skew of the a/c clock, the customer needs to take it into account when the timing is converged, leaving a certain margin.



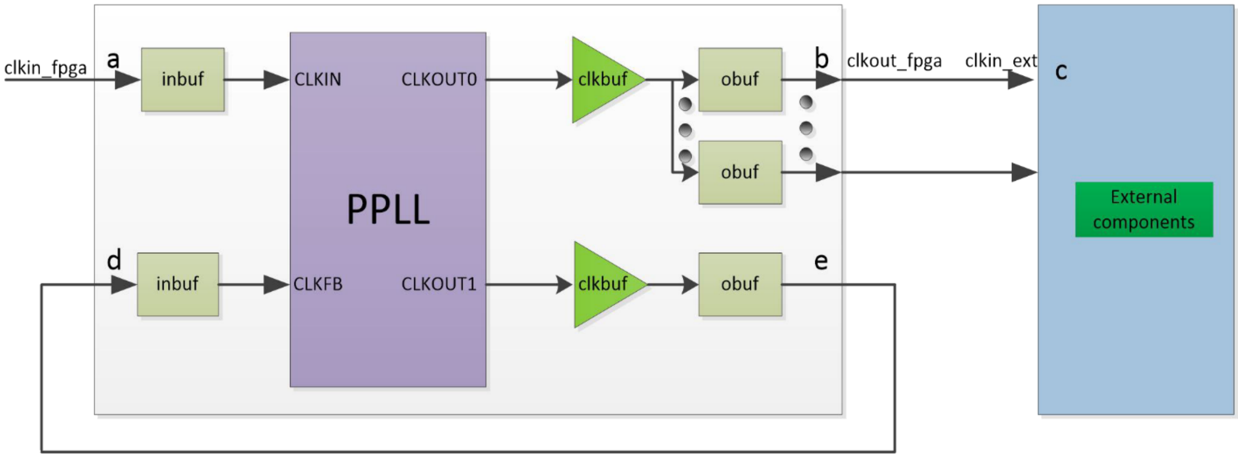


Figure 76 Schematic diagram of PPLL zero delay mode

8.4 Cascading between PPLL

PPLLs can be cascaded. The output interface CLKOUT0~3 is connected to the input reference clock terminal through the PLL clock tree. The frequency selectivity obtained by cascading each other is more. For example, the external input clock frequency is 20MHz. By cascading the first-stage PPLL A 50MHz clock is output as the input of the second-stage PPLL. According to the output frequency calculation formula, the effective output clock frequencies obtained by these two frequencies are different. There is a phase offset between the output clocks of the two PPLLs.

The output frequency cascade formula is as follows:

Cascade output frequency formula: $F_{CLKOUTx} = (\frac{F_{IN} \times MDIV \times FBDIV}{IDIV \times ODIVx})(PPLL1) \times (\frac{MDIV \times FBDIV}{IDIV \times ODIVx})(PPLL2)$

The following two cascading block diagrams are shown:

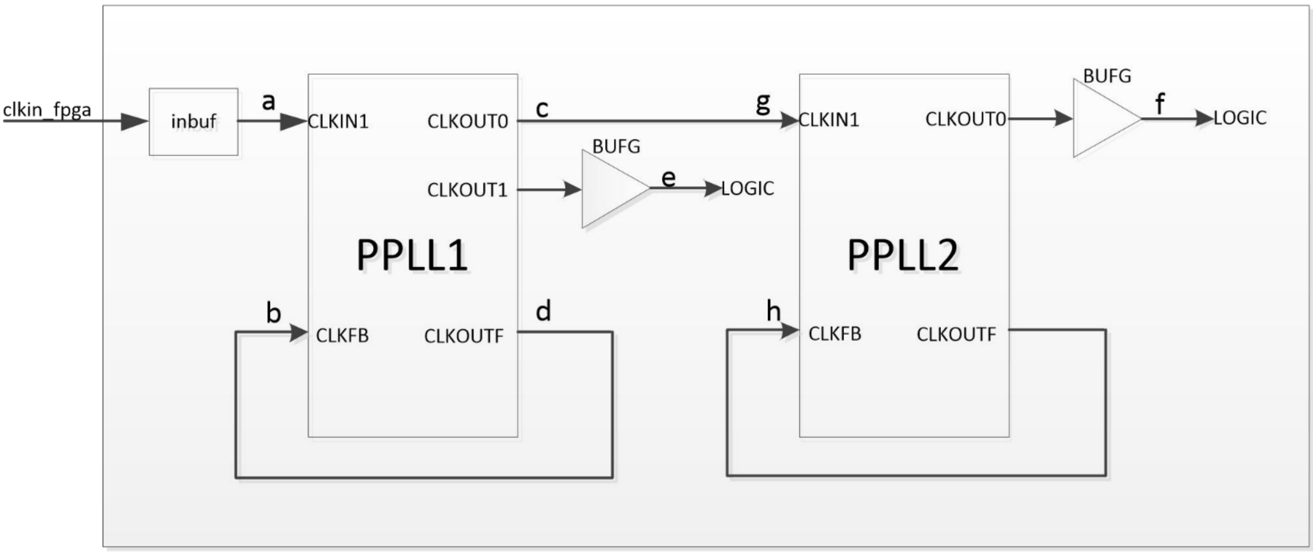


Figure 77 Two PPLL cascade mode 1

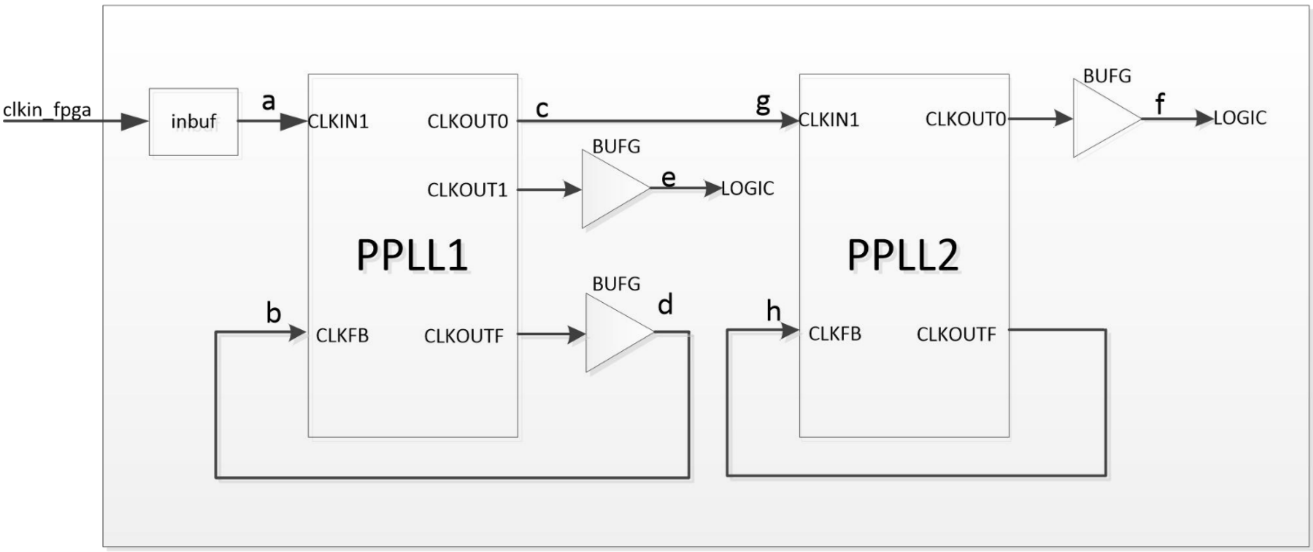


Figure 78 Two PPLL cascade mode 2

Note: PPLL and GPLL can be cascaded.

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